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A Real-Time Neural Spike Based Data Reduction Platform

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Introduction: The research presented was motivated by a long term goal of monitoring the electrical activity of thousands of neurons, in an effort to decipher the brain activity. Recording thousands of neural signals may provide some insight in what Santiago Ramón y Cajal, called "the impenetrable jungle where many investigators have lost themselves"[1]. Monitoring the dynamic signals of thousands of neurons by increasing the number of recording channels in Micro-electrode-Arrays (MEAs) [2] is a breakthrough that might bridge the gap between the firing of neurons and motion, perception or even decision making. Increasing the number of recording channels, real-time data reduction becomes essential to limit the storage memory and transmission rate. Sending spike APs instead of raw data can achieve a data reduction ratio of 0.025 [3]. We present the design of a neural spike-based data reduction platform that can handle thousands of channels on Field Programmable Gate Arrays (FPGAs), making use of their massive parallel processing capabilities.

Material, Methods and Results: The Neural Spike Detection platform receives time division multiplexed serial samples from a high number of neural recording channels at the multi-gigabit receiver port of the FPGA. The receiver performs de-serialization of the data and ensures correct sample-word alignment. The system affiliates each sample to its source channel and performs spike detection. If a spike is detected the spike waveform along with its time stamp and channel ID are passed to an output buffer. The main building block of the design is a spike-based data reduction unit that handles 128 channels [4]. Although, the amount of data is significantly reduced, the system needs to integrate a high-speed communication link to transfer the AP waveforms to the host PC, accounting for transmission bottlenecks during periods of multi-channel neuron bursting [3]. A PCI express link limits queuing-based transmission latencies and saves queue memory during synchronized neuronal activity. The PCIe transmission was applied using a Xillybus IPcore [5].

The design was implemented on a Xilinx® Virtex-5 XUPV5-LX110T FPGA evaluation board and internal signals were monitored using Xilinx ChipScope. The scheduling process for data transmission among the channels was controlled by a Finite-State-Machine. The queue depth was monitored by sending it along with the spike data to the host PC. It was then extracted from the spike data and examined in MATLAB.

It was found that the maximum hardware usage percentage was for the BRAM. Each channel occupied 1120 bits. For the available FPGA boards, the MGTs can handle the maximum number of channels that can be handled by one chip based on the BRAM availability. The design bottleneck is the transmission through PCIe to a host PC at neuronal bursting activities. Further reduction will be needed to decrease the output data, for example by implementing spike sorting in hardware as well.

Discussion: The spike-based data reduction platform can be integrated with a data acquisition system at the interface to the Analog-to-Digital Converters ADCs, that represent the final stage of any neural signal acquisition system. A series of JESD standards have set a common language between fast high performance ADC and FPGAs making use of the high bandwidths SerDes can provide. Theoretically speaking, available ADC with MGTs can handle up to 10,000 recording channels sampled at 25 KSPS.

Significance: This research presented found solutions to some of the problems related to designing a real-time neuronal data reduction platform that can handle thousands of recording channels. It has integrated the application of MGT and autonomous data control to avoid interrupt latencies.

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