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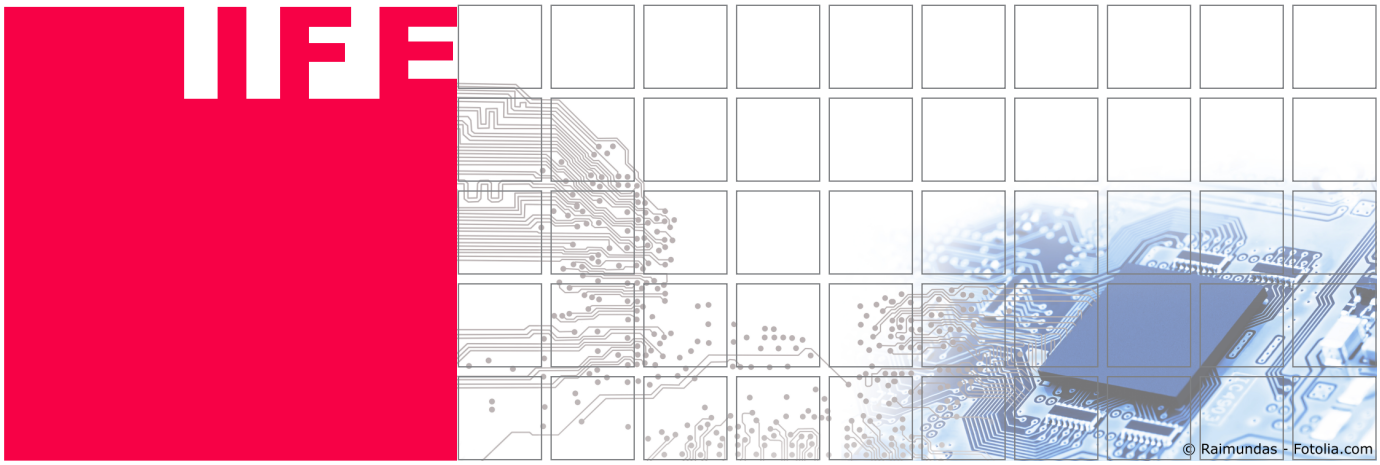

IC Design Fundamentals Practical

Analog Simulation

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10 November, 2020

Contents

1 Buffer Stage

The typical properties of MOS transistor circuits are to be investigated by simulation. The most important properties are:

- **Rise** t_r and **fall times** t_f (between 10 % and 90 % of signal levels, see Figure 2).
  The different characteristics of p- and n-channel transistors are of importance here.
- **Delay times** t_p (at 50 % of the signal level, see Figure 2).
  The most important factors are the transistor parameters and capacitances, whereby the number of stages connected in series is also important (Figure 2 shows an inverter).
- **Current and power consumption** of individual parts of a circuit.
  Special attention should be paid to dynamic conditions compared to static ones.
- **Gate currents**.
  These are determined by the transistor parameters.

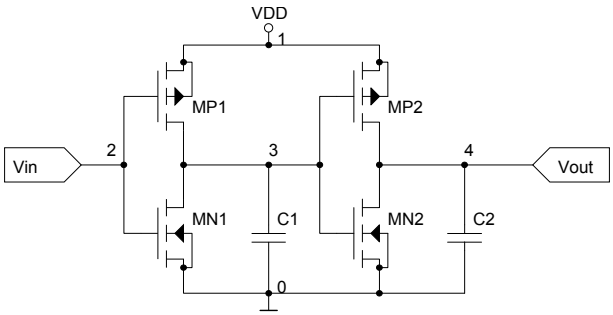

Figure 1: Schematic of a buffer stage.

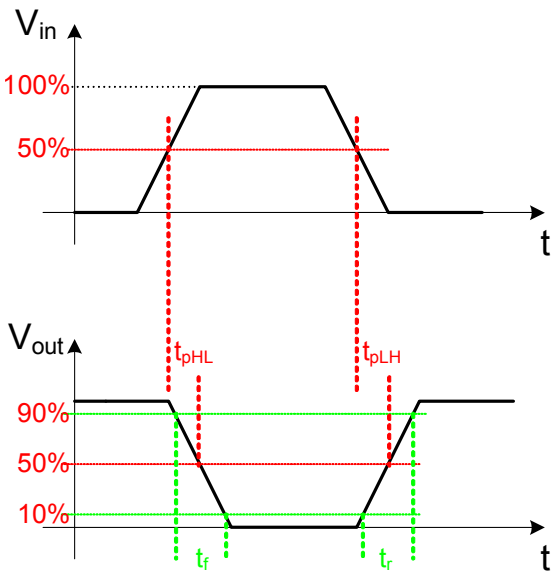

Figure 2: Definition of rise t_r, fall t_f and delay times t_p.

2 Exercise Details

The directory ~ ▸ **hspice** (in your home directory) contains the file **puffer_is2.sp**. It includes the netlist (see Listing 1 on the next page) of the schematic that is shown in Figure 1 on the preceding page. Additionally the file **is2.lib**, which contains the model descriptions of the used MOS transistors, is located there. The first task ist to change the parameters of the transistors (width W and length L), so that the rise and fall times at the output (at 200 fF load capacitance) are approximately the same and are each less than 1 ns.
Furthermore the following points for the determined parameters have to be investigated by appropriate simulations:

- Delay times t_{pLH} and t_{pHL}.
- DC voltage analysis for $0\,\mathrm{V} < V_{in} < 5\,\mathrm{V}$ for the drain currents of the transistors (**I1(MP1)**, **I1(MN1)**, **I1(MP2)** and **I1(MN2)**), as well as the voltages at the nodes **2**, **3** and **4**.
- Power Dissipation in the two output transistors `(V(1)-V(4))*I3(MP2)` and `(V(4))*I1(MN2)` by means of DC voltage analysis and transient analysis. Which part of the power dissipation (cross current or charging/discharging current) is dominant)?
- Gate current of transistor **MP2** (**I2(MP2)**).

```
* Buffer Stage

.OPTIONS post ACCT OPTS accurate
.include is2.lib

MN1 3 2 0 0 MODN W=10u L=3u
MP1 3 2 1 1 MODP W=10u L=3u
MN2 4 3 0 0 MODN W=10u L=3u
MP2 4 3 1 1 MODP W=10u L=3u

C1 3 0 100fF
C2 4 0 200fF

VDD 1 0 DC 5V

VIN 2 0 PWL (0n 0 1n 0 2n 5 4n 5 5n 0 7n 0 8n 5 10n 5 11n 0 13n 0)

.DC VIN 0V 5V .1V

.TRAN 0.01ns 13ns
.OP

.probe  i1(MP1),i1(MN1),i1(MP2),i1(MN2)
.probe  i3(MP1),i3(MN1),i3(MP2),i3(MN2)
.probe  i2(MP1),i2(MN1),i2(MP2),i2(MN2)

.END
```

Listing 1: Netlist for buffer.

3 NOR Gate

In this part a NOR gate is designed and simulated. Therefore the following tasks should be performed.

- A SPICE netlist should be created for the NOR gate, that is shown in Figure 3, whereas the same MOS transistor models should be used as in the previous example.
- The input variables have to be defined in such a way, that the entire function of the gate can be checked in a simulation time of 50 ns. The edge steepness should be 2.5 $\frac{V}{ns}$.
- The transistor parameters should be selected such that a rise and fall time of the output signal of less than 2 ns is realised (for a load capacitance **`C1`** of 500 fF). Pay attention that the symmetry of the times remains and the space requirements are small. What is the problem here?
- The gate delay times shall be determined for all input signal combinations.
- What does the circuit of a NAND gate in CMOS technology look like? Which ratios of the widths of n- and p-channel transistors would you expect for symmetrical rise and fall times?

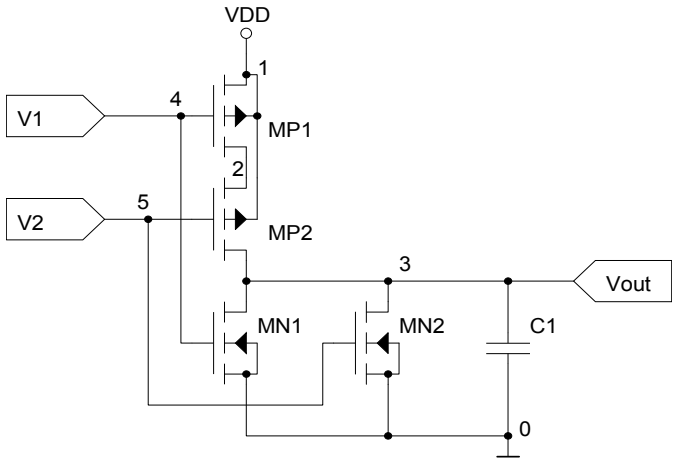

Figure 3: Schematic of NOR-gate.

4 Operational Amplifier

In this part an operational amplifier should be designed with MOS transistors, as shown in Figure 4. In order to increase clarity, parasitic capacitances of the layout are not displayed.

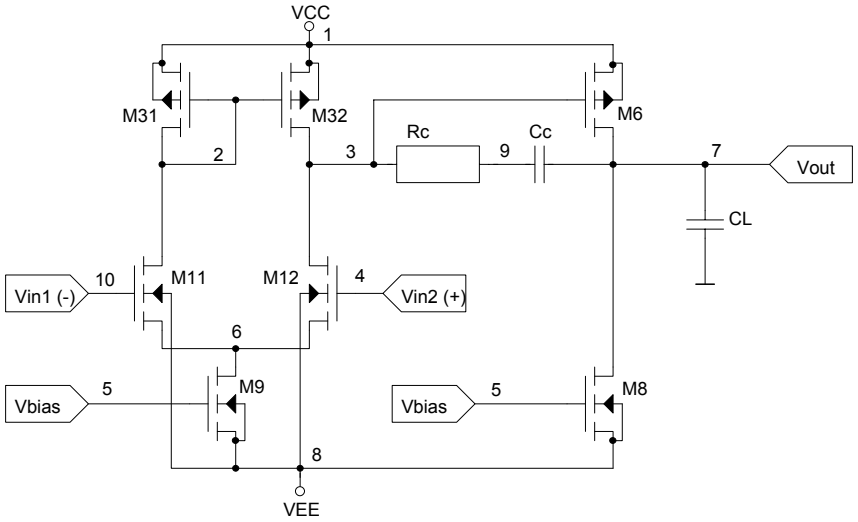

Figure 4: Schematic of operational amplifier.

The following values have to be determined for this circuit by simulation with HSPICE.

- Maximum $\frac{\mathrm{d}V_{out}}{\mathrm{d}t}$ slew rate of the output voltage with and without frequency response correction (**Rc**, **Cc**).
- Bode diagram of the open loop amplifier with and without frequency response correction. From this diagram the differential mode gain A_{DM}, the transit frequency f_T and the phase reserve $\alpha = 180° - |\varphi(f_T)|$ can be found.
- The offset voltage V_0. How does the offset voltage change depending on the geometrical differences of the transistors **M11** and **M12** (varying the width of one transistor)? What is therefore important in the manufacturing of such an operational amplifier?
- The common mode rejection ratio $CMRR = \frac{A_{DM}}{A_{CM}}$.

Furthermore the following points should be examined.

- The transient response of the operational amplifier connected as a follower and as a non-inverting amplifier at different, freely selectable, gains.
- Using a DC analysis, the voltages at the inner nodes should be looked at. Furthermore you should determine the common mode input range in which the operational amplifier is working properly. Therefore you should sweep the interconnected inputs over the whole supply voltage range.

The SPICE netlist for the operational amplifier (from Figure 4) is shown in Listing 2 on the following page. The file is located in ~ ▸ `hspice` ▸ **`op_is2.sp`**.

```
* CMOS-OPAMP

.OPTIONS post ACCT OPTS accurate

M11 2 10 6 8 MODN L=2.5u W=28.19u
M12 3  4 6 8 MODN L=2.5u W=28.19u
M31 2  2 1 1 MODP L=1.3u W=4.04u
M32 3  2 1 1 MODP L=1.3u W=4.04u
M6  7  3 1 1 MODP L=1.3u W=38.49u
M8  7  5 8 8 MODN L=2.5u W=25.38u
M9  6  5 8 8 MODN L=2.5u W=5.21u

.model MODN nmos vto=1.2  kp=35u tox=40n lambda=0.018827
.model MODP pmos vto=-1.2 kp=12u tox=40n lambda=0.018827

VCC 1 0  5V
VEE 8 0 -5V
VIN1 10 0 DC 0V
VIN2  4 0 AC 1 0 PWL(0 0 10n 0 20n 200m)
VBIAS 5 8 2.215V

CL 7 0 8pF
CC 7 9 8pF
RC 9 3 2.53k

.dc VIN2 -0.5mV 0.5mV 0.025m
.ac dec 100 10 1G
.op
.tf v(7) VIN1
.tran 1ns 10us
.probe ac vdb(7)
.end
```

Listing 2: Netlist for operational amplifier.

5 D-Latch

In this part a D-latch is investigated. It is shown in Figure 5. First the input signals should be set in a way, that the correct function of the circuit can be checked. The edge steepness of the input signals should be set by 2.5 $\frac{V}{ns}$.

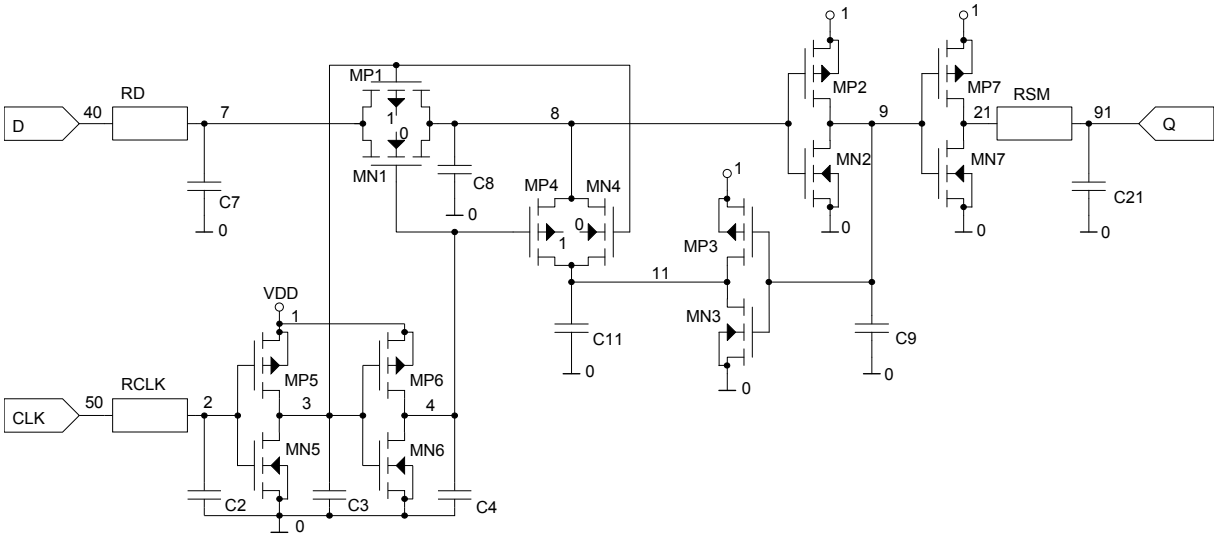

Figure 5: Schematic of D-latch.

The following points should be examined.

- The rise and fall time of the output signal at a load capacitance of 500 fF.
- The delay times $t_{p,CLK,Q}$ from **`CLK`** to **`Q`** and $t_{p,D,Q}$ from **`D`** to **`Q`**.
- The hold time t_H.
- The current consumption of the circuit **`I(VDD)`**.
- The power-on behaviour of the output **`Q`** for various input signal transients when applying the supply voltage.

The SPICE netlist of the D-latch from Figure 5 is shown in Listing 3 on the next page and located in ~ ▸ `hspice` ▸ **`dl_is2.sp`**. It was obtained by extracting the circuit from the layout of a standard cell. For this reason it contains some parasitic components and the specification of area drain (AD), area source (AS), perimeter drain (PD) and perimeter source (PS) for the transistors.

```
* Latch with CLK, D und Q

.OPTIONS post ACCT OPTS accurate
.include is2.lib

* Important Nodes:  CLK ... 50
*                     D ... 40
*                     Q ... 91

MN1  8  4  7  0   MODN  W=7U  L=3U AS=56P   AD=31.5P   PD=16U   PS=30U
+NRS=1.143   NRD=0.643
MP1  8  3  7  1   MODP  W=7U  L=3U AS=56P   AD=31.5P   PD=16U   PS=30U
+NRS=1.143   NRD=0.643
MP2  9  8  1  1   MODP  W=20U L=3U AS=84.5P AD=84.5P   PD=45U   PS=45U
+NRS=9.25    NRD=5.25
MN2  9  8  0  0   MODN  W=8U  L=3U AS=30P   AD=30P     PD=16U   PS=16U
+NRS=4.13    NRD=0.8
MP3 11  9  1  1   MODP  W=20U L=3U AS=37.5P AD=37.5P   PD=19U   PS=19U
+NRS=9.25    NRD=0.5
MN3 11  9  0  0   MODN  W=8U  L=3U AS=30P   AD=30P     PD=16U   PS=16U
+NRS=4.13    NRD=0.8
MN4  8  3 11  0   MODN  W=7U  L=3U AS=30P   AD=31.5P   PD=16U   PS=16U
+NRS=0.643   NRD=0.643
MP4  8  4 11  1   MODP  W=7U  L=3U AS=37.5P AD=31.5P   PD=16U   PS=19U
+NRS=0.643   NRD=0.643
MP5  3  2  1  1   MODP  W=20U L=3U AS=160P  AD=160P    PD=56U   PS=56U
+NRS=0.4     NRD=0.4
MN5  3  2  0  0   MODN  W=10U L=3U AS=80P   AD=80P     PD=36U   PS=36U
+NRS=0.8     NRD=0.8
MP6  4  3  1  1   MODP  W=20U L=3U AS=160P  AD=160P    PD=56U   PS=56U
+NRS=0.3     NRD=0.4
MN6  4  3  0  0   MODN  W=10U L=3U AS=89P   AD=89P     PD=50U   PS=50U
+NRS=0.8     NRD=0.4
MP7 21  9  1  1   MODP  W=50U L=3U AS=400P  AD=400P    PD=116U  PS=116U
+NRS=0.14    NRD=0.16
MN7 21  9  0  0   MODN  W=20U L=3U AS=160P  AD=160P    PD=56U   PS=56U
+NRS=0.325   NRD=0.4

* Internal Capacitances (Layout)

C3   3 0 0.0396460PF
C4   4 0 0.0293765PF
C7   7 0 0.0356125PF
C8   8 0 0.0111660PF
C9   9 0 0.0121125PF
C11 11 0 0.0015600PF
C21 91 0 0.5PF    * Load at the output Q of the D-Latch
C2   2 0 0.0449153PF

* Input and Output Resistances

RD   40  7 50
RCLK 50  2 50
R5M  21 91 1K

* Voltages

VCLK 50 0
VD   40 0
VDD   1 0 DC 5V

.tran 0.1ns 100ns
.op

.end
```

Listing 3: Netlist for D-latch.

6 Simulation of Process Parameter Fluctuations

Simulate the transfer and output characteristics of an **NMOS (**W = **10 µm,** L = **1.2 µm)** and a PMOS for the three characteristic process parameters: typical mean (tm), worst case speed (ws), worst case power (wp). Determine the transconductance from the transfer characteristic and the output conductance from the output characteristic.

The process parameters are given by different transistor models that are available in the library file **cae_params.lib**. The model **MODN_TM** describes the model for an NMOS for the typical mean process parameters. Display the effect of process parameter fluctuations on the characteristics in one panel each.

Furthermore vary the temperature between 0 °C and 75 °C and determine the fluctuation range of the drain current for one operating point (OP) in dependance of temperature and process variations.

7 HSPICE Quick Start Guide

The SPICE program that is installed on the workstations at the Institute of Electronics (IFE) is called HSPICE (Synopsys®). HSPICE is an analog simulator, that is well maintained and widely used in the semiconductor industry.
The whole package can be loaded by the following command.

```
is@felesx:~$ source /tools/env_hspice
```

In addition to the core program, which performs the actual simulation, the workstations also offer a graphical user interface for displaying the netlist elements and the simulation results. The graphical user interface can be started by the following instruction.

```
is@felesx:~$ sx &
```

The basic usage of **sx** is shown in a demonstration at the beginning of the exercises.
The circuits simulated with HSPICE in this exercise are mostly available as SPICE netlist in text form. Therefore the netlists can be edited with any text editor. The files are marked with the file extension ***.sp**.
The circuit is simulated by the following programm call.

```
is@felesx:~$ hspice -i [netlist].sp -o [netlist].lis
```

The output file **[netlist].lis** is logfile containing information on the last simulation run and any messages on errors and warnings that occurred during the simulation.
The simulation results are stored in separate files depending on the type of analysis. The meaning of the file extensions is shown in Table 1. Multiple result files belonging to the same netlist can be identified by consecutive numbering, this is indicated by *. These can come up if the simulation of a netlist is e.g. performed for different temperatures.

File Extension	Results of...
sw*	DC analysis
ac*	AC analysis
tr*	transient analysis

Table 1: File extensions according to analysis type.

7.1 Syntax of SPICE Netlist

Finally some hints on the syntax of SPICE are given. The first line of each SPICE input file is considered the netlist name, has no further meaning and can be treated as a comment. It is important to note that SPICE is case insensitive.

7.1.1 MOS Transistors

transistors have the following syntax.

```
Mxxx drain gate source bulk MODN parameter ; n-channel
Mxxx drain gate source bulk MODP parameter ; p-channel
```

Where **MODN** and **MODP** are the models used for the exercises. These models are described in ~ ▸ hspice ▸ **is2.lib**. Besides the adjusting the length L and the width W (both in meters), there are also many more parameters available, depending on the used level. For details see the HSPICE User's Manual).

7.1.2 Signal sources

For voltage sources the following instruction has to be used.

```
Vxxx node1 node2 DC volt AC volt phase
+ PWL (t1 v1 t2 v2 ...) [PULSE (v1 v2 tp tr tf pw per)]
```

A voltage source is created between `node1` and `node2`. The `DC`, `AC` and `PWL` or `PULSE` statements can be used or omitted as required. `PWL` indicates a voltage in the form of straight lines connecting the point pairs `tx vx` (time, voltage). `PULSE (v1 v2 tp tr tf pw per)` supplies a periodic signal with the voltage levels `v1` and `v2`. The time course is determined by the delay time `td`, the rise and fall time `tr` and `tf`, the time `pw` in which the voltage `v2` is output and the period `per`. In addition, further transient signal forms are possible, when using the corresponding syntax. For more detailed information, please refer to the SPICE syntax.

7.1.3 Scientific Prefix Abbreviations

The abbreviations for scientific prefixes are shown in Table 2. As SPICE is case insensitive, there needs to be a possibility to distinguish milli with mega. For this reasons mega is assigned the abbreviation **meg** or **x**.

Abbreviation	Multiplier	Name	Abbreviation	Multiplier	Name
m	10^{-3}	milli	**k**	10^{3}	kilo
u	10^{-6}	micro	**meg, x**	10^{6}	mega
n	10^{-9}	nano	**g**	10^{9}	giga
p	10^{-12}	pico	**t**	10^{12}	tera
f	10^{-15}	femto			

Table 2: SPICE abbreviations for scientic prefixes.

7.1.4 Analysis Statements

In the following the syntax of the most important analysis instructions is given.

- **`.DC`** `var start stop incr`
  DC analysis: A voltage sweep from `start` to `stop` ist performed in steps of `incr` at the voltage source `var`.
- **`.AC`** `type points fstart fstop`
  AC analysis: Depending on the `type` (`LIN` for linear, `DEC` for dec. logarithmic) the frequency of all AC sources is swept from `fstart` to `fstop`, whereby the number of measured values is indicated by `points`. For `DEC` the value is given per decade. The AC voltage is specified by the AC source instruction `var node1 node2 AC volt phase`.
- **`.OP`**
  Operating point calculation: The DC operating point of the circuit is calculated. The results are only visible in the results file `*.lis` and can not be graphically annotated.
- **`.TF`** `out in`
  Transfer function: The transfer function (gain) is calculated from `in` to `out` (e.g.: **`.TF`** `V(8)`**`VIN`**). By this also the input resistance at `in` and the output resistance at `out` are calculated. The result is only visible in the results file `*.lis`.
- **`.TRAN`** `inc stop`
  Transient analysis: The time is increased in steps of `inc` up to the `stop` value. This analysis evaluates the transient part of a signal source, such as `PWL` (piecewise linear) or `PULSE`.

7.1.5 Temperature

For performing more simulations with different temperatures, the following command can be used.

```
.TEMP temp1 temp2 ...
```

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