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Analysis of a Transistor Amplifier Circuit

Large- and Small-Signal Analysis and Magnitude and Phase Response of a PNP Common-Base-Circuit

published by

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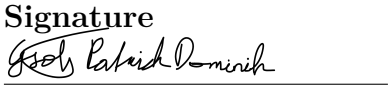
Patrick Dominik Gsöls		Graz, 29.03.2020

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Abstract

Transistor circuits play an important role in electronics. That's why good knowledge of basic transistor circuits is essential for every electrical engineering student, because those circuits build a fundamental basis for more complex transistor circuits. Transistors are almost used everywhere in nowadays electronic. Transistors can be used as either switches or amplifiers. Consequently, there are several methods for analysing and designing such electronic circuits.

The aim of this document is to guide students through the analysis of a bipolar junction transistor amplifier circuit. The circuit analysis will focus on a pnp-common-base transistor circuit. The circuit analysis concepts, which will be shown in this document, can be applied analogously to the two remaining basic transistor amplifier circuits. All analysis concepts are as well valid for the analysis of a field effect transistor amplifier circuit and more complex circuit topologies. The only difference between field-effect transistor and bipolar junction transistor circuits is the control mode (field-effect transistors are voltage controlled). The main focus of the analysis will be on calculating the bias points, input and output resistance, phase inversion, voltage gain and magnitude and phase response of the circuit. Undoubtedly, there are several ways of calculation which lead to the same result. Therefore, this work highlights two different analysis concepts for the small-signal analysis and two for analysing the frequency behaviour of the circuit. For the small-signal analysis the conventional and the node-voltage method is introduced. Furthermore, the frequency behaviour analysis is introduced by a conventional method and the method of quadrupoles.

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1. The PNP-Common-Base Circuit

The chosen circuit to be analysed is depicted in Figure 1. The given circuit is pnp-common-base transistor circuit. We want to analyse the large signal and small-signal behaviour as well as the input resistance, the output resistance and the voltage gain of the circuit. The aim of this documentation is to describe two different ways to analyse such a transistor amplifier. The intent is to perform a conventional network analysis with meshes and nodes (Kirchhoff's Law) as well as the node voltage method. Furthermore, the frequency and phase response of the circuit are getting determined.

1.1. Circuit Explanation

Let's have a more detailed look on the circuit in Figure 1. The circuit is called common-base, because the base terminal represents here for ac-signals, the common terminal for the input and output signal. The capacitor C_B forces the base of the transistor Q for ac-signals to ground potential (gnd). U_{Bat} symbolises the power supply of the circuit. The resistors R_1 and R_2 are setting the bias point of the circuit. Due to the biasing the collector current I_C is defined by the collector resistance R_C and the emitter resistance R_E. R_E is basically used for biasing purpose and ensures that current I_E has path where it can flow. Otherwise the input source u_G has to produce the biasing. u_G and the the corresponding resistance R_G are representing a waveform-generator. The collector current I_C has an impact on the transconductance g_m of the circuit, which is shown in section 3.2. Furthermore, the transconductance influences the differential collector-emitter r_{CE} and base-emitter r_{BE} resistance, which is dependent on the operating point. These resistances in interaction with R_E, R_C and R_L will influence the voltage gain of the circuit. This is evident in section 3.7. The capacitors C_{in} and C_{out} are used for decoupling. Furthermore, the arrow at the emitter is representing the current direction.

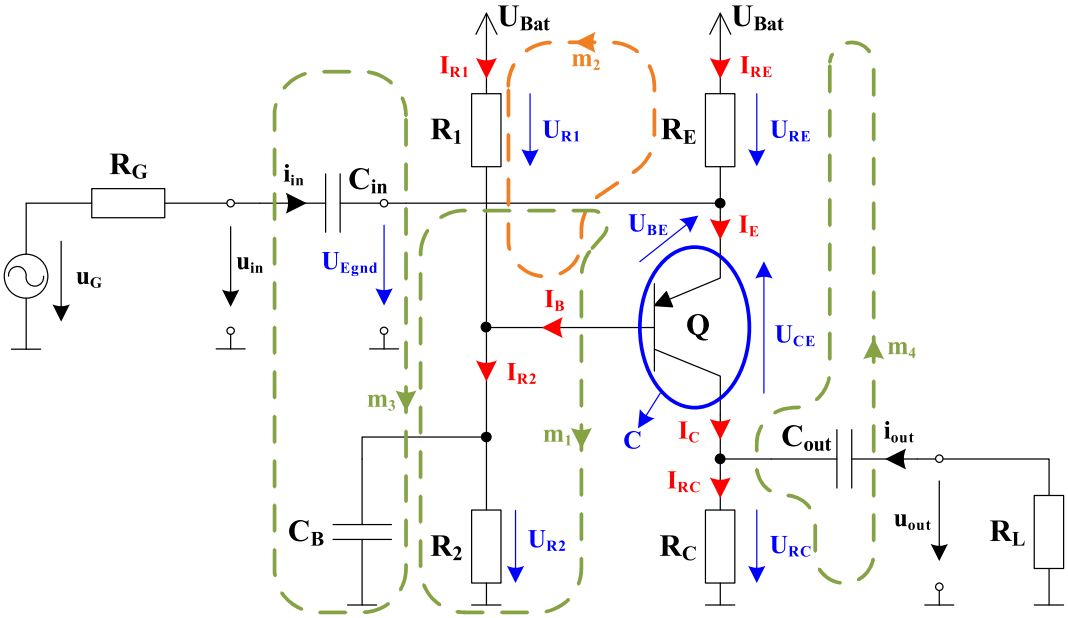

Figure 1: PNP-Common-Base-Circuit

1.2. Circuit Data

The transistor Q, which is used for this application, is a general purpose transistor ($BC557B$). The transistor specifications are listed below.

- $U_{BE} = -0.7\ V$
- $U_{CEsat} = -0.3\ V$
- $U_{EA} = -20\ V$ (early-voltage[1])
- $B = 350$
- $T = 300\ K$

All values of the components, shown in Figure 1, are listed below.

- $U_{Bat} = 9\ V$
- $R_1 = 320\ \Omega$
- $R_2 = 1.8\ k\Omega$
- $R_E = 150\ \Omega$
- $R_C = 380\ \Omega$
- $R_L = 1\ k\Omega$
- $R_G = 50\ \Omega$
- $C_{in} = 100\ \mu F$
- $C_{out} = 20\ \mu F$
- $C_B = 47\ \mu F$

1.3. Advantages of the Common-Base Circuit

The common-base amplifier ...

- is a non-inverting amplifier stage [2].
- has similar voltage gain and output terminal impedance as the common-emitter stage [2].
- has compared to the common-emitter and common-collector stage no Miller-Multiplication[2]. That's why common-base circuits are used for RF-applications [6].
- has compared to the common-emitter and common-collector stage a very low input impedance. This property is useful for RF-applications e.g. an antenna-LNA-interfaces (LNA - low noise amplifier), because antennas usually have low impedance. So with this property it is possible to achieve pretty simple impedance matching between the antenna and amplifier [7, p. 272].

[1] If the early-voltage U_{EA} is not given, it is computable via the concept of the appendix section A.
[2] The Miller-Multiplication is described in the appendix section D.

2. Large-Signal Analysis (Bias Point)

The aim of the large-signal analysis is to find the operating point **OP** of the circuit [2]. The large-signal analysis is an important step in circuit analysis because with the knowledge of the operating point it is possible to calculate the small-signal parameters, which is shown in section 3. With these parameters the non-linear circuit can be broken down into a linear network which can be easily calculated with usage of linear circuit analysis concepts.

2.1. Large-Signal Model

The large-signal model of a BJT in forward active mode can be established as follows. The terminal between base and emitter can be modelled by a diode. For this diode a known equation namely the Shockley-Equation exists (see equation 1). The current, which is flowing between the collector and emitter terminal, can be modelled by either a current controlled current source or a voltage controlled current source. The control parameter is either the current through the base-emitter diode or the voltage over the diode. The large-signal model of a npn is given in Figure 2. The model for a pnp only differs in the current directions (inverse current direction).

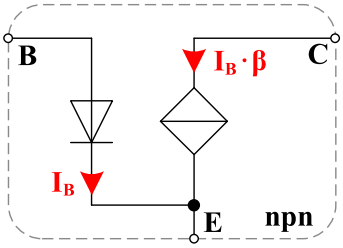

Figure 2: Large-signal model

2.2. Large-Signal Equations for Arbitrary Bias Points

Due to the fact that a BJT is formed out of two pn-junctions it is obvious that the diode equation (Shockley-Equation) has to appear [2, p. 97]. The forward current is given by

$$I_D = I_S \cdot \left(e^{\frac{U_D}{U_T}} - 1 \right) \tag{1}$$

Where U_T is the temperature voltage. The temperature voltage is defined by

$$U_T = \frac{k \cdot T}{q} \tag{2}$$

For easier hand-calculations later on in the small-signal analysis (see section 3) a simplified version of the large-signal equations, which are derivable from the complex Gummel-Poon model [8], is used (see Table 1). Due to accuracy reasons and small-signal parameter calculation the Early-Effect is included (second order effect). The equations are valid for the forward active region ($|U_{CE}| > |U_{CEsat}|$).

Table 1: Simplified large-signal equations of the **BJT**

npn	***pnp***
$I_B = \frac{I_S}{B} \cdot e^{\frac{U_{BE}}{U_T}}$	$I_B = \frac{I_S}{B} \cdot e^{\frac{\lvert U_{BE}\rvert}{U_T}}$
$I_C = I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)$	$I_C = I_S \cdot e^{\frac{\lvert U_{BE}\rvert}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)$
$I_E = I_C + I_B$	$I_E = I_C + I_B$

To get a better understanding of the above depicted equations, shown in Table 1, for the npn and pnp transistor, the current and voltage counting-arrows are shown in Figure 3 and 4 below. By looking to the above depicted equations of the npn-transistor, it is visible that there is no sign difference between current and voltage. This is due to the same orientation of the counting-arrows. On the contrary, for the pnp transistor there exists a sign difference between current and voltage. Therefore, the absolute value of the voltages has been taken in the above depicted equations. We could get rid of the absolute values by changing the direction of the voltage counting-arrows.

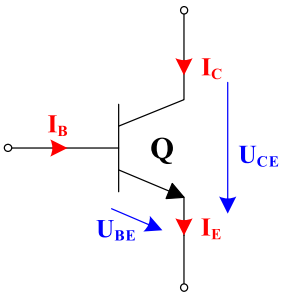

Figure 3: NPN-transistor

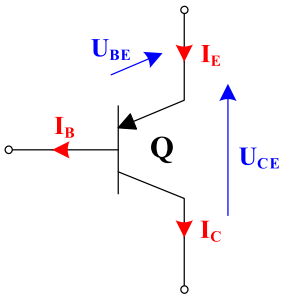

Figure 4: PNP-transistor

To determine the bias point of the circuit, it is useful and still accurate if a further simplification is done. For this kind of analysis, it is quite common to neglect the Early-Voltage. The simplified equations are depicted in Table 2 below.

Table 2: Simplified large-signal equations for bias point determination

npn	***pnp***
$I_B = \frac{I_S}{B} \cdot e^{\frac{U_{BE}}{U_T}}$	$I_B = \frac{I_S}{B} \cdot e^{\frac{\lvert U_{BE}\rvert}{U_T}}$
$I_C = I_S \cdot e^{\frac{U_{BE}}{U_T}} = B \cdot I_B$	$I_C = I_S \cdot e^{\frac{\lvert U_{BE}\rvert}{U_T}} = B \cdot I_B$
$I_E = I_C + I_B$	$I_E = I_C + I_B$

2.3. The Large-Signal Concept in Action

The first step for analysing a transistor circuit is to determine the large signal behaviour (Bias Points). We assume that there is no input signal at the input terminal of the circuit shown in Figure 1. With the large-signal analysis, the DC-operating point of the circuit is calculated.

Let's start with a few assumptions. First, we will assume that the base current is much smaller than the current through the base-biasing resistors R_1 and R_2.

$$|I_B| < \left|\frac{I_{R2}}{10}\right| \Rightarrow I_{R1} \approx I_{R2} \tag{3}$$

Furthermore, the transistor has to stay in the linear or forward active operating region to ensure amplification [9]. In the linear region the current stays almost constant.

$$|U_{CE}| > |U_{CEsat}| \tag{4}$$

Because the current through resistor R_2 is approximately the same as the current through resistor R_1, we can derive the voltages as for an unloaded voltage divider. So the voltage U_{R2} over the resistor R_2 can be easily calculated.

$$U_{R2} = U_{Bat} \cdot \frac{R_2}{R_1 + R_2} = 9\ V \cdot \frac{1.8\ k\Omega}{320\ \Omega + 1.8\ k\Omega} = 7.642\ V \tag{5}$$

Out of U_{R2} the voltage U_{R1} can be calculated be applying Kirchhoff's Law.

$$U_{R1} = U_{Bat} - U_{R2} = 9\ V + 7.642\ V = 1.358\ V \tag{6}$$

Mesh m_1, shown in Figure 1, provides the relation for the emitter-ground voltage U_{Egnd}.

$$\begin{aligned} m_1: \quad & -U_{R2} + U_{BE} + U_{Egnd} = 0\ V \\ \Leftrightarrow \quad & U_{Egnd} = U_{R2} - U_{BE} = 7.642\ V - (-0.7\ V) = 8.342\ V \end{aligned} \tag{7}$$

Mesh m_2, shown in Figure 1, provides the relation for the voltage U_{RE} over the emitter resistor.

$$\begin{aligned} m_2: \quad & U_{R1} + U_{BE} - U_{RE} = 0\ V \\ \Leftrightarrow \quad & U_{RE} = U_{R1} + U_{BE} = 1.358\ V + (-0.7\ V) = 658.49\ mV \end{aligned} \tag{8}$$

The current through the resistor R_E is given by the following relation:

$$I_{RE} = \frac{U_{RE}}{R_E} = \frac{658.49\ mV}{150\ \Omega} = 4.39\ mA \tag{9}$$

Because we perform the large-signal analysis upon the circuit (Bias Point) there is no current flowing in and out of the input (where the waveform generator is connected) and output (where the load is connected) terminals of the circuit shown in Figure 1. So we get for the current I_E, which is flowing into the emitter of the transistor, the following result:

$$I_E = I_{RE} = 4.39\ mA \tag{10}$$

After analysing node C, which encloses the transistor, we get the following node equation:

$$\begin{aligned} C: \quad & -I_E + I_C + I_B = 0\ A \quad \Leftrightarrow \quad -I_E + B \cdot I_B + I_B = 0\ A \\ \Leftrightarrow \quad & I_B = \frac{I_E}{1+B} = \frac{4.39\ mA}{1+350} = 12.507\ \mu A \end{aligned} \tag{11}$$

To ensure that the assumption of I_B (see equation 3) was correct, the equation needs to be tested by values.

$$|I_B| < \left|\frac{I_{R2}}{10}\right| = \left|\frac{U_{R2}}{R_2 \cdot 10}\right| \quad \Leftrightarrow \quad |12.507\ \mu A| < |424.56\ \mu A| \quad \text{q.e.d} \tag{12}$$

By using the relation between the collector I_C and the base current I_B the collector current can be expressed as follows, if the transistor is in the linear operating region [10, p. 309]:

$$I_C = B \cdot I_B = 350 \cdot 12.507\ \mu A = 4.377\ mA \tag{13}$$

Because we perform the large signal analysis of the circuit (Bias Point) there is no current flowing in and out of the input (where the waveform generator is connected) and output (where the load is connected) terminals of the circuit shown in Figure 1. So we get for the current I_{RC}, which is flowing through resistor R_C, the following result:

$$I_{RC} = I_C = 4.377\ mA \tag{14}$$

The voltage over the resistor R_C is then given by:

$$U_{RC} = I_{RC} \cdot R_C = 4.377\ mA \cdot 380\ \Omega = 1.663\ V \tag{15}$$

Mesh m_3, shown in Figure 1, provides the relation for the collector-emitter voltage U_{CE}.

$$\begin{aligned} m_3: \quad & U_{Bat} - U_{RC} + U_{CE} - U_{RE} = 0\ V \\ \Leftrightarrow \quad & U_{CE} = U_{RC} + U_{RE} - U_{Bat} = 1.663\ V + 658.49\ mV - 9\ V = -6.678\ V \end{aligned} \tag{16}$$

To ensure that the transistor is really in the linear operating region, equation 4 needs to be tested by values. This would also be the last step of the large signal analysis.

$$|U_{CE}| > |U_{CEsat}| \quad \Leftrightarrow \quad |-6.678\ V| > |-0.3\ V| \quad \text{q.e.d} \tag{17}$$

2.3.1. Calculated Operating Point Values

This section gives a brief overview of the calculated bias point values. Table 3 below shows the calculated voltage DC-points.

Table 3: Calculated voltage DC-points

Component	***Resistor***				***Transistor***	
Variable	U_{R1}	U_{R2}	U_{RE}	U_{RC}	U_{Egnd}	U_{CE}
OP Values	1.358 V	7.642 V	658.49 mV	1.663 V	8.342 V	-6.678 V

Analogous to the voltage DC-points, the current DC-points are shown in Table 4 below.

Table 4: Calculated current DC-points

Component	***Resistor***		***Transistor***		
Variable	I_{RE}	I_{RC}	I_E	I_B	I_C
OP Values	4.390 mA	4.377 mA	4.390 mA	12.507 μA	4.377 mA

3. Small-Signal Analysis and Corresponding Parameters

For studying the response of a circuit regarding to a small signal changes, we use the small signal analysis.

The small signal analysis computes quantities such as the voltage gain and input/output impedances. It is important to bear in mind that the small-signal analysis deals with only small changes in voltages and currents in a circuit and their quiescent values [5, p. 176].

The small-signal analysis is basically a tool for linearisation in a specific point (operating point ***OP*** of the circuit). So we don't have to deal with the non-linear Shockley-Equation of the BJT any more, which would cause more complex calculations.

The reason why we do the linearisation is because we want to calculate the behaviour of a linear network. This property gives the advantage that linear network analysis tools, like the nodal voltage analysis or superposition principle, can be used. Be aware that this linearisation is only valid for a small range of signal changes, so it has marginal effect on our previously calculated operating point (see section 2). Transistors have a non-linear relation between the input and output if we see it as electric quadrupole. With the small signal parameters we can calculate the slope of each operating point in the set of characteristic curves of the transistor. We will calculate the small signal parameters for the operating point which we got in section 2.

3.1. Small-Signal Model

The derivation of the small-signal model from the large-signal counterpart is relatively straightforward. We perturb the voltage difference between every two terminals (while the third terminal remains at a constant potential), determine the changes in the currents flowing through all terminals, and represent the results by proper circuit elements such as controlled current sources or resistors (see Figure 5) [5, p. 140].

The model for a pnp only differs in the direction of the base and collector current.

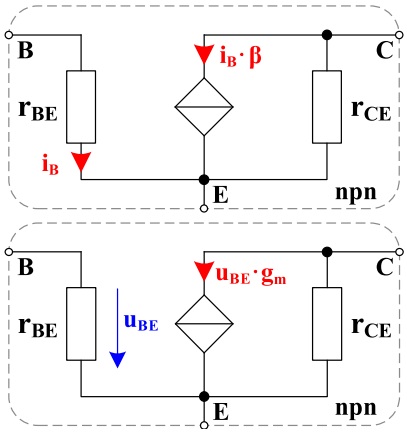

Figure 5: Small-signal model

3.2. Transconductance

The transconductance g_m describes the differential change of the collector current i_C depending on the base-emitter voltage u_{BE}. The transconductance is a rate for how the base-emitter voltage influences the collector current. This relationship is depicted in equation 18 below.

$$\begin{aligned} g_m &= \left.\frac{\partial i_C}{\partial u_{BE}}\right|_{OP} = \frac{\partial I_C}{\partial U_{BE}} = \frac{\partial}{\partial U_{BE}}\left(I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)\right) \\ &= \frac{1}{U_T} \cdot \underbrace{I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)}_{I_C} = \frac{I_C}{U_T} \overset{(2)}{=} \frac{q \cdot I_C}{k \cdot T} \\ &= \frac{1.602 \cdot 10^{-19}\ C \cdot 4.377\ mA}{1.381 \cdot 10^{-23}\ \frac{J}{K} \cdot 300\ K} = 169.388\ mS \end{aligned} \tag{18}$$

3.3. Small-Signal Current Gain

The small-signal current gain β describes the differential change of the collector current i_C depending on the base current i_B. The small signal current gain is an amplification factor between collector and base current.

By the use of the equation for the base I_B and collector current I_C (see Table 1) it is possible to substitute I_S. After applying this substitution the equation will be free of the saturation reverse current I_S.

$$\begin{aligned} &I_B = \frac{I_S}{B} \cdot e^{\frac{U_{BE}}{U_T}} \Leftrightarrow I_S = I_B \cdot B \cdot e^{-\frac{U_{BE}}{U_T}} \\ &I_C = I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right) = I_B \cdot B \cdot \underbrace{e^{-\frac{U_{BE}}{U_T}} \cdot e^{\frac{U_{BE}}{U_T}}}_{=1} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right) = I_B \cdot B \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right) \end{aligned} \tag{19}$$

With the relationship from above (see equation 19) the small-signal current gain can be expressed as follows:

$$\beta = \left.\frac{\partial i_C}{\partial i_B}\right|_{OP} = \frac{\partial I_C}{\partial I_B} = \frac{\partial}{\partial I_B}\left(I_B \cdot B \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)\right) = B \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right) \approx B = 350 \tag{20}$$

3.4. Small-Signal Base-Emitter Resistance

The small-signal base-emitter resistance r_{BE} describes the differential change of the base-emitter voltage u_{BE} depending on the base current i_B. This relationship is depicted in equation 21 below.

$$r_{BE} = \left.\frac{\partial u_{BE}}{\partial i_B}\right|_{OP} \tag{21}$$

By rearranging equation 20 the differential change of the base-current ∂i_B can be expressed via the following equation:

$$\beta = \left.\frac{\partial i_C}{\partial i_B}\right|_{OP} \quad \Leftrightarrow \quad \partial i_B = \left.\frac{\partial i_C}{\beta}\right|_{OP} \tag{22}$$

Finally, the base-emitter resistance r_{BE}, from equation 21, can be calculated by using the chain rule for derivatives and plugging in the known equations from the previous sections 3.3 and 3.2.

$$\begin{aligned} r_{BE} &= \left.\frac{\partial u_{BE}}{\partial i_B}\right|_{OP} = \left.\frac{\partial u_{BE}\left(i_C\left(i_B\right)\right)}{\partial i_B}\right|_{OP} = \left.\frac{\partial u_{BE}}{\partial i_C}\right|_{OP} \cdot \left.\frac{\partial i_C}{\partial i_B}\right|_{OP} \overset{(22)}{=} \beta \cdot \left.\frac{\partial u_{BE}}{\partial i_C}\right|_{OP} \\ &\overset{(18)}{=} \left.\frac{\beta}{g_m}\right|_{OP} \overset{(20)}{\approx} \frac{B}{g_m} = \frac{B}{\frac{I_C}{U_T}} = \frac{B \cdot U_T}{I_C} \overset{(2)}{=} \frac{B \cdot k \cdot T}{I_C \cdot q} \\ &= \frac{350 \cdot 1.381 \cdot 10^{-23}\ \frac{J}{K} \cdot 300\ K}{4.377\ mA \cdot 1.602 \cdot 10^{-19}\ C} = 2.066\ k\Omega \end{aligned} \tag{23}$$

3.5. Small-Signal Collector-Emitter Resistance

The small-signal collector-emitter resistance r_{CE} describes the differential change of the collector-emitter voltage u_{CE} depending on the collector current i_C. This relationship is depicted in equation 24 below.

$$r_{CE} = \left.\frac{\partial u_{CE}}{\partial i_C}\right|_{OP} \tag{24}$$

To derive an equation for the collector-emitter resistance equation 24 first needs to be rearranged.

$$r_{CE} = \left.\frac{\partial u_{CE}}{\partial i_C}\right|_{OP} = \frac{1}{g_{CE}} \quad \Leftrightarrow \quad g_{CE} = \left.\frac{\partial i_C}{\partial u_{CE}}\right|_{OP} \tag{25}$$

The relationship for the collector-emitter conductance g_{CE} can be derived by plugging in the equation for the collector-current I_C (see Table 1) and a few equivalent transformations.

$$\begin{aligned}
g_{CE} &= \left.\frac{\partial i_C}{\partial u_{CE}}\right|_{OP} = \frac{\partial I_C}{\partial U_{CE}} = \frac{\partial}{\partial U_{CE}}\left(I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)\right) \\
\Leftrightarrow \quad g_{CE} &= 0 + I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \frac{1}{U_{EA}} = I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \frac{1}{U_{EA}} \cdot \frac{\left(1 + \frac{U_{CE}}{U_{EA}}\right)}{\left(1 + \frac{U_{CE}}{U_{EA}}\right)} \\
&= \underbrace{I_S \cdot e^{\frac{U_{BE}}{U_T}} \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)}_{I_C} \cdot \left(\frac{1}{U_{EA}}\right) \cdot \left(1 + \frac{U_{CE}}{U_{EA}}\right)^{-1} = I_C \cdot \frac{\frac{1}{U_{EA}}}{\left(1 + \frac{U_{CE}}{U_{EA}}\right)} \\
&= I_C \cdot \frac{\frac{1}{U_{EA}}}{\frac{U_{EA}+U_{CE}}{U_{EA}}} = \frac{I_C}{U_{EA} + U_{CE}} = \frac{1}{r_{CE}}
\end{aligned} \tag{26}$$

To get the equation for the collector-emitter resistance r_{CE}, we have to form the reciprocal of the equation above.

$$g_{CE} = \frac{I_C}{U_{EA} + U_{CE}} = \frac{1}{r_{CE}} \quad \Leftrightarrow \quad r_{CE} = \frac{1}{g_{CE}} = \begin{cases} \dfrac{U_{EA} + U_{CE}}{I_C} & \text{for} \quad U_{CE},\ U_{EA} \geq 0 \\ - \dfrac{U_{EA} + U_{CE}}{I_C} & \text{for} \quad U_{CE},\ U_{EA} < 0 \end{cases} \tag{27}$$

To ensure that equation 27 is valid for **npn** and **pnp** devices the absolute value is taken.

$$r_{CE} = \left|\frac{U_{EA} + U_{CE}}{I_C}\right| = \left|\frac{-20\ V + (-6.678\ V)}{4.377\ mA}\right| = 6.094\ k\Omega \tag{28}$$

3.6. Small-Signal Equivalent Circuit

With the knowledge of the small-signal parameters from section 3.2 to 3.5 and the small-signal model of a pnp transistor, which is shown in section 3.1, it is possible to redraw the circuit from Figure 1 to get the small-signal equivalent circuit, which is depicted in Figure 6.

Also important to mention is that the capacitors (decoupling capacitors) are replaced by shorts, because the capacitances are selected in such a manner so that the corresponding reactances are neglectable for the frequency for which the circuit is designed. Also important to bear in mind is that the circuit contains two voltages sources. On the one hand there is the supply voltage U_{Bat}, which is necessary for biasing, and on the other hand there is the signal source u_G. As mentioned in section 3, the small signal parameters are used for linearisation. Due to that, the super-position-principle can be applied onto the circuit. So only the signal changes are getting analysed. The supply voltage U_{Bat} is turned-off.

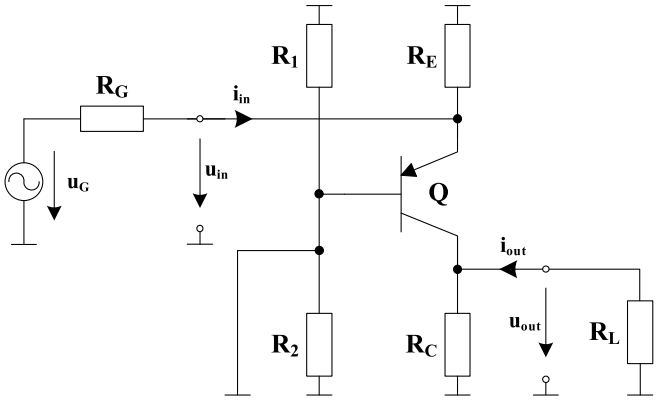

Figure 6: Small-signal circuit

Finally, the transistor Q is replaced by the small-signal model for a pnp transistor, which is shown in Figure 7. After successful calculation of the small-signal behaviour it can be merged with the large-signal behaviour. The merged result will be the overall behaviour of the pnp-common-base circuit. So we have a combination of DC- and AC-signals between the decoupling capacitors C_{in} and C_{out}.

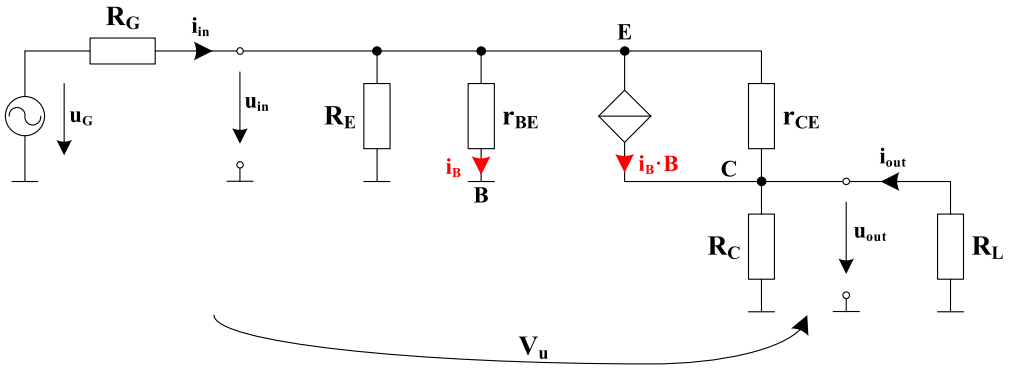

Figure 7: Small-signal equivalent circuit

3.7. Conventional Network Analysis Method with Meshes and Nodes

The aim of the conventional network analysis method is to determine the input/output terminal resistance as well as the voltage gain of the circuit. The equivalent circuit shown in Figure 8 below is copied over from the previous page, but extended by meshes, cut-sets and currents.

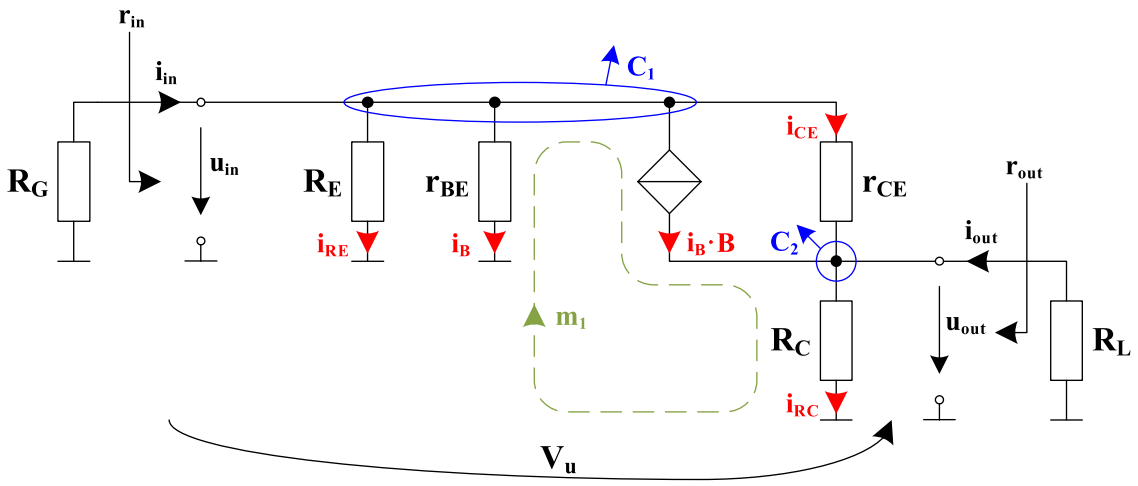

Figure 8: Circuit for the conventional network analysis

To determine the input terminal impedance/resistance r_{in} a voltage is applied at the input terminal, which is shown in Figure 9. Furthermore, the circuit for calculating r_{in} can also be used for calculating the voltage gain of the amplifier stage. For that, the output voltage is monitored while manipulating the input voltage. For calculating the output terminal impedance/resistance r_{out}, it is the other way around (see Figure 10). Bear in mind that for calculating the output terminal impedance/resistance r_{out} of the amplifier circuit, shown in Figure 8, the input voltage source is set to zero [5].

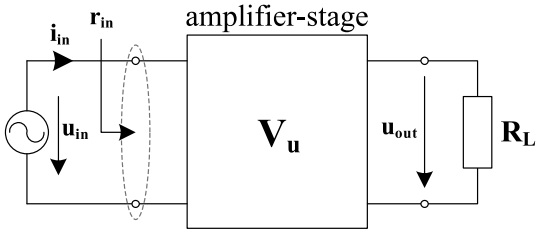

Figure 9: Input-terminal impedance

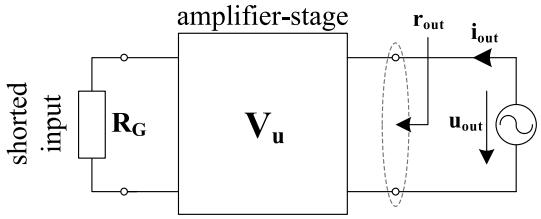

Figure 10: Output-terminal impedance

Out of the small-signal equivalent circuit of Figure 8 the mesh and node equations can be derived as

$$\begin{aligned} C_1\text{:}&\ -i_{in}+i_{RE}+i_B+i_B\cdot B+i_{CE}=0\ A\\ C_2\text{:}&\ -i_B\cdot B-i_{CE}+i_{RC}-i_{out}=0\ A\\ m_1\text{:}&\ -u_{in}+u_{CE}+u_{out}=0\ V \quad\Leftrightarrow\quad u_{CE}=u_{in}-u_{out} \end{aligned} \tag{29}$$

3.7.1. Small-Signal Voltage Gain

As next step the node voltages are plugged into the second current node equation C_2 (see equation 29).

$$C_2: \quad -i_B\cdot B-i_{CE}+i_{RC}-i_{out}=-\frac{u_{in}}{r_{BE}}\cdot B-\frac{u_{CE}}{r_{CE}}+\frac{u_{out}}{R_C}-\left(-\frac{u_{out}}{R_L}\right)=0\ A \tag{30}$$

The current node equation 30 from above has still one unknown part included namely the collector-emitter voltage u_{CE}. By usage of the mesh equation m_1 (see equation 29) the unknown collector-emitter voltage can be replaced by a known term.

$$C_2: \quad 0\ A=-\frac{u_{in}}{r_{BE}}\cdot B-\frac{u_{in}-u_{out}}{r_{CE}}+\frac{u_{out}}{R_C}+\frac{u_{out}}{R_L} \tag{31}$$

By separating and rearrangement of equation 31 the small-signal voltage gain can be expressed by

$$\begin{aligned} C_2:&\quad u_{in}\cdot\left(\frac{B}{r_{BE}}+\frac{1}{r_{CE}}\right)=u_{out}\cdot\left(\frac{1}{r_{CE}}+\frac{1}{R_C}+\frac{1}{R_L}\right)\\ \Leftrightarrow&\quad \frac{u_{out}}{u_{in}}=V_u=\left(\frac{B}{r_{BE}}+\frac{1}{r_{CE}}\right)\cdot\left(\frac{1}{r_{CE}}+\frac{1}{R_C}+\frac{1}{R_L}\right)^{-1}\\ \Leftrightarrow&\quad V_u=\frac{u_{out}}{u_{in}}=\left(\frac{350}{2.066\ k\Omega}+\frac{1}{6.094\ k\Omega}\right)\cdot\left(\frac{1}{6.094\ k\Omega}+\frac{1}{380\ \Omega}+\frac{1}{1\ k\Omega}\right)^{-1}=44.68 \end{aligned} \tag{32}$$

3.7.2. Input Terminal Resistance

For expressing the input terminal resistance r_{in} through the input current i_{in} and the input voltage u_{in} the first node equation C_1 (see equation 29) is used. Because we want known parameters in our node current equation the currents are getting replaced by the voltage drop over the resistors.

$$C_1\colon\ -i_{in} + i_{RE} + i_B \cdot (B+1) + i_{CE} = -i_{in} + \frac{u_{in}}{R_E} + \frac{u_{in}}{r_{BE}} \cdot (B+1) + \frac{u_{CE}}{r_{CE}} = 0\ A \tag{33}$$

After a few equivalent transformations and plugging in the mesh equation m_1 (see equation 29), the input current i_{in} is derived with respect to the input voltage u_{in} and the input terminal resistance r_{in}.

$$\begin{aligned} C_1:\quad & i_{in} = \frac{u_{in}}{R_E} + \frac{u_{in}}{r_{BE}} \cdot (B+1) + \frac{u_{in} - u_{out}}{r_{CE}} = \frac{u_{in}}{R_E} + \frac{u_{in}}{r_{BE}} \cdot (B+1) + \frac{u_{in} - V_u \cdot u_{in}}{r_{CE}} \\ \Leftrightarrow\quad & i_{in} = u_{in} \cdot \underbrace{\left(\frac{1}{R_E} + \frac{B+1}{r_{BE}} + \frac{1-V_u}{r_{CE}}\right)}_{\frac{1}{r_{in}}} = \frac{u_{in}}{r_{in}} \end{aligned} \tag{34}$$

Rearranging equation 34 delivers the final result for the input terminal resistance r_{in}.

$$r_{in} = \frac{u_{in}}{i_{in}} = \frac{1}{\frac{1}{R_E} + \frac{B+1}{r_{BE}} + \frac{1-V_u}{r_{CE}}} = \frac{1}{\frac{1}{150\ \Omega} + \frac{350+1}{2.066\ k\Omega} + \frac{1-44.68}{6.094\ k\Omega}} = 5.903\ \Omega \tag{35}$$

3.7.3. Output Terminal Resistance

Analogous to the input terminal resistance r_{in}, the output terminal resistance r_{out} can be expressed through the output current i_{out} and the output voltage u_{out}. By using the first current node equation C_1 (see equation 29) and plugging in all voltage drops over the resistors, an expression for the input voltage u_{in} can be derived.

$$\begin{aligned} C_1:\quad & -i_{in} + i_{RE} + i_B + i_B \cdot B + i_{CE} = \frac{u_{in}}{R_G} + \frac{u_{in}}{R_E} + \frac{u_{in}}{r_{BE}} \cdot (B+1) + \frac{u_{CE}}{r_{CE}} = 0\ A \\ \Leftrightarrow\quad & 0\ A \overset{(29)}{=} \frac{u_{in}}{R_G} + \frac{u_{in}}{R_E} + \frac{u_{in}}{r_{BE}} \cdot (B+1) + \frac{u_{in} - u_{out}}{r_{CE}} \\ \Leftrightarrow\quad & 0\ A = u_{in} \cdot \left(\frac{1}{R_G} + \frac{1}{R_E} + \frac{B+1}{r_{BE}} + \frac{1}{r_{CE}}\right) - u_{out} \cdot \left(\frac{1}{r_{CE}}\right) \\ \Leftrightarrow\quad & u_{in} \cdot \underbrace{\left(\frac{1}{R_G} + \frac{1}{R_E} + \frac{B+1}{r_{BE}} + \frac{1}{r_{CE}}\right)}_{\alpha} = u_{out} \cdot \underbrace{\left(\frac{1}{r_{CE}}\right)}_{\delta} \\ \Leftrightarrow\quad & u_{in} = \frac{u_{out} \cdot \delta}{\alpha} \end{aligned} \tag{36}$$

Next, the second current node equation C_2 is used. There all currents are getting replaced by the voltage drops over the resistors, too. After a few equivalent transformations and plugging in the input voltage u_{in}, which was calculated on the previous page (see equation 36), an expression for the output current i_{out} appears.

$$
\begin{aligned}
C_2: \quad & -i_B \cdot B - i_{CE} + i_{RC} - i_{out} = -\frac{u_{in}}{r_{BE}} \cdot B - \frac{u_{CE}}{r_{CE}} + \frac{u_{out}}{R_C} - i_{out} = 0\ A \\
\Leftrightarrow \quad & 0\ A = -\frac{u_{in}}{r_{BE}} \cdot B - \frac{u_{in} - u_{out}}{r_{CE}} + \frac{u_{out}}{R_C} - i_{out} \\
\Leftrightarrow \quad & 0\ A = -u_{in} \cdot \underbrace{\left(\frac{B}{r_{BE}} + \frac{1}{r_{CE}}\right)}_{\varepsilon} + u_{out} \cdot \underbrace{\left(\frac{1}{r_{CE}} + \frac{1}{R_C}\right)}_{\gamma} - i_{out} = -u_{in} \cdot \varepsilon + u_{out} \cdot \gamma - i_{out} \\
\Leftrightarrow \quad & i_{out} \overset{(36)}{=} -\frac{u_{out} \cdot \delta}{\alpha} \cdot \varepsilon + u_{out} \cdot \gamma = u_{out} \cdot \underbrace{\left(\gamma - \frac{\delta \cdot \varepsilon}{\alpha}\right)}_{\frac{1}{r_{out}}} = \frac{u_{out}}{r_{out}}
\end{aligned}
\tag{37}
$$

After rearranging equation 37 we get the equation for the output terminal resistance r_{out}.

$$
\begin{aligned}
r_{out} = \frac{u_{out}}{i_{out}} = \frac{1}{\gamma - \frac{\delta \cdot \varepsilon}{\alpha}} &= \frac{1}{\frac{1}{R_C} + \frac{1}{r_{CE}} - \frac{\frac{1}{r_{CE}} \cdot \left(\frac{B}{r_{BE}} + \frac{1}{r_{CE}}\right)}{\frac{1}{R_G} + \frac{1}{R_E} + \frac{B+1}{r_{BE}} + \frac{1}{r_{CE}}}} \\
\Leftrightarrow \quad r_{out} &= \frac{1}{\frac{1}{380\ \Omega} + \frac{1}{6.094\ k\Omega} - \frac{\frac{1}{6.094\ k\Omega} \cdot \left(\frac{350}{2.066\ k\Omega} + \frac{1}{6.094\ k\Omega}\right)}{\frac{1}{50\ \Omega} + \frac{1}{150\ \Omega} + \frac{350+1}{2.066\ k\Omega} + \frac{1}{6.094\ k\Omega}}} = 376.76\ \Omega
\end{aligned}
\tag{38}
$$

3.8. Node-Voltage Method

The node-voltage method is a very convenient tool to analyse linear circuits, because all conductances and side conditions are put into a matrix. This matrix can be easily solved by numerical software like Matlab®, Python® or MathCAD®. The main advantage of this method is for sure that we only have to derive the set of equations, which needs to be plugged into a matrix. This analysis method is also suitable for circuits where energy storing components are included. The model we use for the small-signal equivalent circuit (see Figure 5) is greatly simplified. If parasitic capacitors are added to the transistor model, the conventional network analysis method would become way more complicated. So the node-voltage analysis method would fit perfectly for such problems.

3.8.1. Additional Information to the Node-Voltage Method

If the circuit contains dependent sources, the node-voltage equations must be supplemented with the constraint equations (side conditions **CS**) imposed by the presence of the dependent sources [3, p. 95].

Furthermore, the admittance matrix $\underline{\mathbf{Y}}$ of the node-voltage method is extended by the side conditions. Also important to mention is that the control current/voltage of dependent sources is modelled by an extra independent source (see Figure 11 - independent voltage source u_{n3}). This approach gives the advantage that the control current/voltage appears in the solution vector $\vec{S}$.

Finally, the inner matrix of the overall matrix (admittance matrix $\underline{\mathbf{Y}}$) is symmetrical if we use the convention that out-flowing currents are counted with a positive sign and incoming currents are counted with a negative sign. Moreover, the leading diagonal has only conductances with positive signs included. For each node, all to the node connected conductances appear in the corresponding cell of the leading diagonal. The off-diagonal elements are representing the conductances between two adjacent nodes.

3.8.2. Input Terminal Resistance and Voltage Gain

In Figure 11 shows the small-signal equivalent circuit, which is used for the calculation of the input terminal resistance r_{in} and the small-signal voltage gain V_u of the common-base amplifier shown in Figure 1. The circuit below is the same as the small-signal equivalent circuit shown in Figure 7, but with a few modifications for the modified node-voltage method. The voltage source at the input terminal of the circuit is defined by the expression $u_{in} = 0.1V \cdot \sin(2\pi \cdot 1kHz \cdot t)$ (arbitrary value).

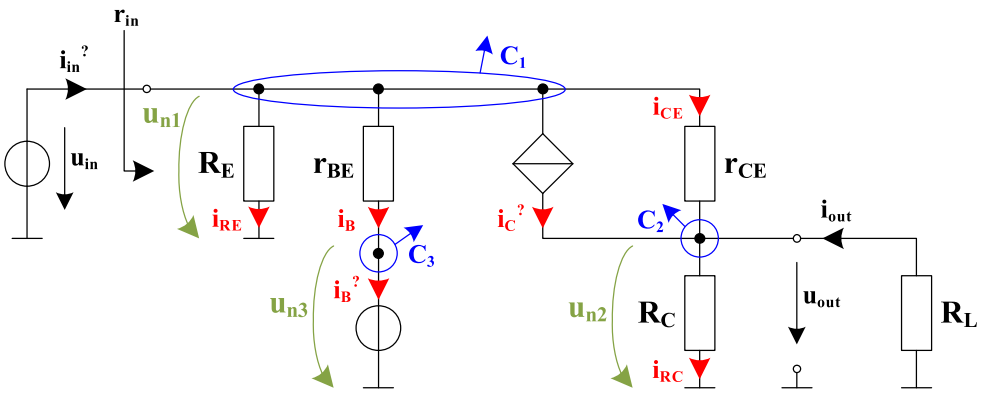

Figure 11: Circuit for calculating the input resistance and voltage gain

The circuit shown in Figure 11 above delivers the set of equations for the current nodes and the side conditions.

$$\begin{aligned}
C_1&: \; -i_{in}^{?} + i_{RE} + i_B + i_C^{?} + i_{CE} = 0\ A \\
C_2&: \; -i_C^{?} - i_{CE} + i_{RC} - i_{out} = 0\ A \\
C_3&: \; -i_B + i_B^{?} = 0\ A \\
SC_1&: \; i_C^{?} = B \cdot i_B^{?} \\
SC_2&: \; u_{n3} = 0\ V \\
SC_3&: \; u_{n1} = u_{in} \;\ldots \text{ arbitrary testing voltage}
\end{aligned} \tag{39}$$

Next, the currents through the resistors are getting expressed by the node-voltages.

$$\begin{aligned}
i_{RE} &= \frac{u_{n1}}{R_E} = u_{n1} \cdot G_E \\
i_{RC} &= \frac{u_{n2}}{R_C} = u_{n2} \cdot G_C \\
i_{CE} &= \frac{u_{n1} - u_{n2}}{r_{CE}} = (u_{n1} - u_{n2}) \cdot g_{CE} \\
i_B &= \frac{u_{n1} - u_{n3}}{r_{BE}} = (u_{n1} - u_{n3}) \cdot g_{BE} \\
i_{out} &= \frac{-u_{n2}}{R_L} = -u_{n2} \cdot G_L
\end{aligned} \tag{40}$$

Now the equation set 39 and 40 can be combined. So the new set of equations (see equation 41) only contains the node voltages u_{ni}, conductances g_i, control parameters (e.g. B) and the unknown currents $i_i^?$. The derived set of equations is now well defined which leads to a solvable set of linear equations.

$$\begin{aligned}
C_1\text{: } & u_{n1} \cdot G_E + (u_{n1} - u_{n3}) \cdot g_{BE} + (u_{n1} - u_{n2}) \cdot g_{CE} - i_{in}^? + i_C^? = 0\ A \\
C_2\text{: } & (u_{n2} - u_{n1}) \cdot g_{CE} + u_{n2} \cdot G_C + u_{n2} \cdot G_L - i_C^? = 0\ A \\
C_3\text{: } & (u_{n3} - u_{n1}) \cdot g_{BE} + i_B^? = 0\ A \\
SC_1\text{: } & -i_C^? + B \cdot i_B^? = 0\ A \\
SC_2\text{: } & u_{n3} = 0\ V \\
SC_3\text{: } & u_{n1} = u_{in}
\end{aligned} \tag{41}$$

After sorting the set of equations 41 depending on the node voltages, we get the following:

$$\begin{aligned}
C_1\text{: } & u_{n1} \cdot (G_E + g_{BE} + g_{CE}) + u_{n2} \cdot (-g_{CE}) + u_{n3} \cdot (-g_{BE}) - i_{in}^? + i_C^? = 0\ A \\
C_2\text{: } & u_{n1} \cdot (-g_{CE}) + u_{n2} \cdot (g_{CE} + G_C + G_L) - i_C^? = 0\ A \\
C_3\text{: } & u_{n1} \cdot (-g_{BE}) + u_{n3} \cdot (g_{BE}) + i_B^? = 0\ A \\
SC_1\text{: } & -i_C^? + B \cdot i_B^? = 0\ A \\
SC_2\text{: } & u_{n3} = 0\ V \\
SC_3\text{: } & u_{n1} = u_{in}
\end{aligned} \tag{42}$$

Next, the circuit can be transformed into the frequency domain. For more information, please read appendix G. This allows to solve the circuit without having to deal with trigonometric functions. By using the transformation equation 100, equation 42 from above, can be rewritten as follows:

$$\begin{aligned}
C_1\text{: } & \underline{U_{n1}} \cdot (G_E + g_{BE} + g_{CE}) + \underline{U_{n2}} \cdot (-g_{CE}) + \underline{U_{n3}} \cdot (-g_{BE}) - \underline{I_{in}^?} + \underline{I_C^?} = 0\ A \\
C_2\text{: } & \underline{U_{n1}} \cdot (-g_{CE}) + \underline{U_{n2}} \cdot (g_{CE} + G_C + G_L) - \underline{I_C^?} = 0\ A \\
C_3\text{: } & \underline{U_{n1}} \cdot (-g_{BE}) + \underline{U_{n3}} \cdot (g_{BE}) + \underline{I_B^?} = 0\ A \\
SC_1\text{: } & -\underline{I_C^?} + B \cdot \underline{I_B^?} = 0\ A \\
SC_2\text{: } & \underline{U_{n3}} = 0\ V \\
SC_3\text{: } & \underline{U_{n1}} = \underline{U_{in}}
\end{aligned} \tag{43}$$

With respect to the transformation equation 100 the input voltage u_{in} can be express as follows:

$$\begin{aligned}
u_{in} &= \hat{U}_{in} \cdot \sin(\omega t + \varphi_u) = \Im\left\{\underline{u_{in}}\right\} = \Im\left\{\hat{U}_{in} \cdot e^{j(\omega t + \varphi_u)}\right\} = \Im\left\{e^{j\omega t} \cdot \underbrace{\hat{U}_{in} \cdot e^{j\varphi_u}}_{\underline{U_{in}}}\right\} \\
&= 0.1V \cdot \sin(2\pi f \cdot t) = \Im\left\{e^{j\omega t} \cdot 0.1V \cdot e^{j0}\right\} = \Im\left\{e^{j\omega t} \cdot 0.1V \angle \underline{0^\circ}\right\}
\end{aligned} \tag{44}$$

Next, the set of equations from above (see equation 42) can be rewritten as vector-matrix-notation. This is necessary for solving it with a numerical solver.

$$\underbrace{\begin{bmatrix} G_E + g_{BE} + g_{CE} & -g_{CE} & -g_{BE} & -1 & 1 & 0 \\ -g_{CE} & g_{CE} + G_C + G_L & 0 & 0 & -1 & 0 \\ -g_{BE} & 0 & g_{BE} & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 & B \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}}_{\underline{\mathbf{Y}}} \cdot \begin{bmatrix} \underline{U_{n1}} \\ \underline{U_{n2}} \\ \underline{U_{n3}} \\ \underline{I_{in}^{?}} \\ \underline{I_C^{?}} \\ \underline{I_B^{?}} \end{bmatrix} = \underbrace{\begin{bmatrix} 0\ A \\ 0\ A \\ 0\ A \\ 0\ A \\ 0\ V \\ \underline{U_{in}} \end{bmatrix}}_{\underline{\vec{S}}} \tag{45}$$

After rearranging equation 45, the set of equations can be solved by values.

$$\underline{\mathbf{Y}} \cdot \begin{bmatrix} \underline{U_{n1}} \\ \underline{U_{n2}} \\ \underline{U_{n3}} \\ \underline{I_{in}^{?}} \\ \underline{I_C^{?}} \\ \underline{I_B^{?}} \end{bmatrix} = \underline{\vec{S}} \quad \Leftrightarrow \quad \begin{bmatrix} \underline{U_{n1}} \\ \underline{U_{n2}} \\ \underline{U_{n3}} \\ \underline{I_{in}^{?}} \\ \underline{I_C^{?}} \\ \underline{I_B^{?}} \end{bmatrix} = \underline{\mathbf{Y}}^{-1} \cdot \underline{\vec{S}} = \begin{bmatrix} 0.1\ V \\ 4.468\ V \\ 0\ V \\ 16.939\ mA \\ 16.941\ mA \\ 48.403\ \mu A \end{bmatrix} \tag{46}$$

Finally, the input terminal resistance r_{in} is calculated out of the input voltage u_{in} and input current $i_{in}^{?}$. This is valid because there are only resistances appearing in the small-signal equivalent circuit. So no phase-shift will appear.

$$r_{in} = \frac{u_{in}}{i_{in}^{?}} = \frac{u_{n1}}{i_{in}^{?}} = \frac{\left|\underline{U_{n1}}\right| \cdot \sin\left(2\pi f \cdot t\right)}{\left|\underline{I_{in}^{?}}\right| \cdot \sin\left(2\pi f \cdot t\right)} = \frac{0.1\ V}{16.939\ mA} = 5.903\ \Omega \tag{47}$$

Moreover, the small-signal voltage gain V_u is the ratio of the output voltage u_{out} with respect to the input voltage u_{in}. Analogous to the input terminal resistance r_{in}, the equation 48 below is valid cause of a complete resistive circuit.

$$V_u = \frac{u_{out}}{u_{in}} = \frac{u_{n2}}{u_{n1}} = \frac{\left|\underline{U_{n2}}\right| \cdot \sin\left(2\pi f \cdot t\right)}{\left|\underline{U_{n1}}\right| \cdot \sin\left(2\pi f \cdot t\right)} = \frac{4.468\ V}{0.1\ V} = 44.68 \tag{48}$$

3.8.3. Output Terminal Resistance

In Figure 12 below is the circuit depicted which is used for the calculation of the output terminal resistance of the common-base amplifier, which is shown in Figure 1. The circuit below is the same as the small-signal equivalent circuit of Figure 7, but with a few modifications for the modified node-voltage method. The voltage source at the output terminal of the circuit is defined with $u_{out} = 10V \cdot \sin(2\pi \cdot 1kHz \cdot t)$ (arbitrary value).

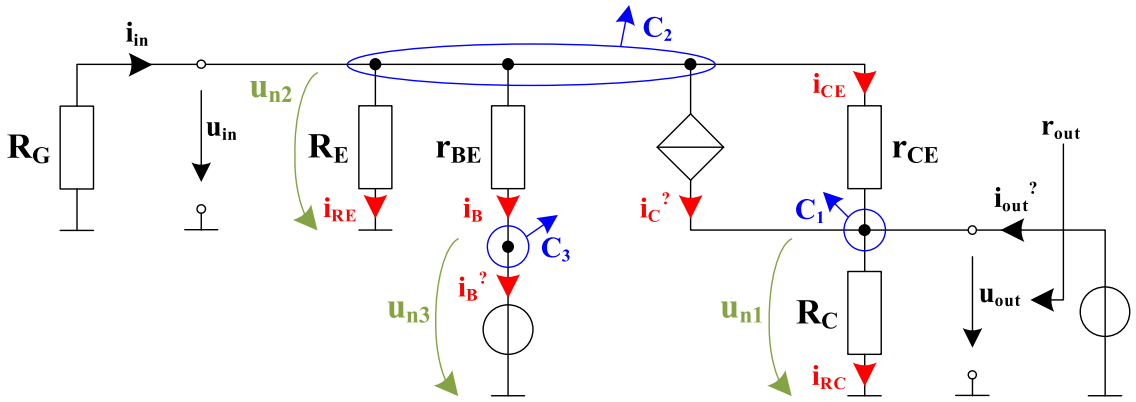

Figure 12: Circuit for calculating the output resistance

The circuit shown in Figure 12 above delivers the set of equations for the current nodes and the side conditions.

$$\begin{aligned}
C_1&: \; -i_{out}^{?} + i_{RC} - i_{CE} - i_C^{?} = 0\ A \\
C_2&: \; -i_{in} + i_{RE} + i_B + i_C^{?} + i_{CE} = 0\ A \\
C_3&: \; -i_B + i_B^{?} = 0\ A \\
SC_1&: \; u_{n1} = u_{out} \;\ldots \text{ arbitrary testing voltage} \\
SC_2&: \; u_{n3} = 0\ V \\
SC_3&: \; i_C^{?} = B \cdot i_B^{?}
\end{aligned} \tag{49}$$

Next, the currents through the resistors are getting expressed by the node-voltages.

$$\begin{aligned}
i_{RE} &= \frac{u_{n2}}{R_E} = u_{n2} \cdot G_E \\
i_{RC} &= \frac{u_{n1}}{R_C} = u_{n1} \cdot G_C \\
i_{CE} &= \frac{u_{n2} - u_{n1}}{r_{CE}} = (u_{n2} - u_{n1}) \cdot g_{CE} \\
i_B &= \frac{u_{n2} - u_{n3}}{r_{BE}} = (u_{n2} - u_{n3}) \cdot g_{BE} \\
i_{in} &= \frac{-u_{n2}}{R_G} = -u_{n2} \cdot G_L
\end{aligned} \tag{50}$$

Now the equation set 49 and 50 can be combined. So the new set of equations (see equation 51) only contains the node voltages u_{ni}, conductances g_i, control parameters (e.g. B) and the unknown currents $i_i^?$. The derived set of equations is now well defined which leads to a solvable set of linear equations.

$$\begin{aligned}
C_1&: u_{n1} \cdot G_C + (u_{n1} - u_{n2}) \cdot g_{CE} - i_{out}^? - i_C^? = 0\ A \\
C_2&: u_{n2} \cdot G_G + u_{n2} \cdot G_E + (u_{n2} - u_{n3}) \cdot g_{BE} + (u_{n2} - u_{n1}) \cdot g_{CE} + i_C^? = 0\ A \\
C_3&: (u_{n3} - u_{n2}) \cdot g_{BE} + i_B^? = 0\ A \\
SC_1&: u_{n1} = u_{out} \\
SC_2&: u_{n3} = 0\ V \\
SC_3&: i_C^? = B \cdot i_B^?
\end{aligned} \tag{51}$$

After sorting the set of equations 51 depending on the node voltages we get the following:

$$\begin{aligned}
C_1&: u_{n1} \cdot (G_C + g_{CE}) + u_{n2} \cdot (-g_{CE}) - i_{out}^? - i_C^? = 0\ A \\
C_2&: u_{n1} \cdot (-g_{CE}) + u_{n2} \cdot (G_G + G_E + g_{BE} + g_{CE}) + u_{n3} \cdot (-g_{BE}) + i_C^? = 0\ A \\
C_3&: u_{n2} \cdot (-g_{BE}) + u_{n3} \cdot (g_{BE}) + i_B^? = 0\ A \\
SC_1&: u_{n1} = u_{out} \\
SC_2&: u_{n3} = 0\ V \\
SC_3&: -i_C^? + B \cdot i_B^? = 0\ A
\end{aligned} \tag{52}$$

Next, the circuit can be transformed into the frequency domain. For more information, please read appendix G. This allows to solve the circuit without having to deal with trigonometric functions. By using the transformation equation 100, equation 52 from above can be rewritten as follows:

$$\begin{aligned}
C_1&: \underline{U_{n1}} \cdot (G_C + g_{CE}) + \underline{U_{n2}} \cdot (-g_{CE}) - \underline{I_{out}^?} - \underline{I_C^?} = 0\ A \\
C_2&: \underline{U_{n1}} \cdot (-g_{CE}) + \underline{U_{n2}} \cdot (G_G + G_E + g_{BE} + g_{CE}) + \underline{U_{n3}} \cdot (-g_{BE}) + \underline{I_C^?} = 0\ A \\
C_3&: \underline{U_{n2}} \cdot (-g_{BE}) + \underline{U_{n3}} \cdot (g_{BE}) + \underline{I_B^?} = 0\ A \\
SC_1&: \underline{U_{n1}} = \underline{U_{out}} \\
SC_2&: \underline{U_{n3}} = 0\ V \\
SC_3&: -\underline{I_C^?} + B \cdot \underline{I_B^?} = 0\ A
\end{aligned} \tag{53}$$

With respect to the transformation equation 100 the output voltage u_{out} can be express as follows:

$$\begin{aligned}
u_{out} &= \hat{U}_{out} \cdot \sin(\omega t + \varphi_u) = \Im\left\{\underline{u_{out}}\right\} = \Im\left\{\hat{U}_{out} \cdot e^{j(\omega t + \varphi_u)}\right\} = \Im\left\{e^{j\omega t} \cdot \underbrace{\hat{U}_{out} \cdot e^{j\varphi_u}}_{\underline{U_{out}}}\right\} \\
&= 10V \cdot \sin(2\pi f \cdot t) = \Im\left\{e^{j\omega t} \cdot 10V \cdot e^{j0}\right\} = \Im\left\{e^{j\omega t} \cdot 10V \underline{/0^\circ}\right\}
\end{aligned} \tag{54}$$

Next, the set of equations from the previous page (see equation 52) can be rewritten as vector-matrix-notation. This is necessary for solving it with a numerical solver.

$$\underbrace{\begin{bmatrix} G_C + g_{CE} & -g_{CE} & 0 & -1 & -1 & 0 \\ -g_{CE} & G_G + G_E + g_{BE} + g_{CE} & -g_{BE} & 0 & 1 & 0 \\ 0 & -g_{BE} & g_{BE} & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & B \end{bmatrix}}_{\underline{\mathbf{Y}}} \cdot \begin{bmatrix} \underline{U_{n1}} \\ \underline{U_{n2}} \\ \underline{U_{n3}} \\ \underline{I^?_{out}} \\ \underline{I^?_C} \\ \underline{I^?_B} \end{bmatrix} = \underbrace{\begin{bmatrix} 0\ A \\ 0\ A \\ 0\ A \\ \underline{U_{out}} \\ 0\ V \\ 0\ A \end{bmatrix}}_{\underline{\vec{S}}} \tag{55}$$

After rearranging equation 55, the set of equations can be solved by values.

$$\underline{\mathbf{Y}} \cdot \begin{bmatrix} \underline{U_{n1}} \\ \underline{U_{n2}} \\ \underline{U_{n3}} \\ \underline{I^?_{out}} \\ \underline{I^?_C} \\ \underline{I^?_B} \end{bmatrix} = \underline{\vec{S}} \quad \Leftrightarrow \quad \begin{bmatrix} u_{n1} \\ u_{n2} \\ u_{n3} \\ i^?_{out} \\ i^?_C \\ i^?_B \end{bmatrix} = \underline{\mathbf{Y}}^{-1} \cdot \underline{\vec{S}} = \begin{bmatrix} 10\ V \\ 8.341\ mV \\ 0\ V \\ 26.542\ mA \\ 1.413\ mA \\ 4.038\ \mu A \end{bmatrix} \tag{56}$$

Finally, the output terminal resistance r_{out} is calculated out of the output voltage u_{out} and output current $i^?_{out}$. This is valid because there are only resistances appearing in the small-signal equivalent circuit. So no phase-shift will appear.

$$r_{out} = \frac{u_{out}}{i^?_{out}} = \frac{u_{n1}}{i^?_{out}} = \frac{\left|\underline{U_{n1}}\right| \cdot \sin\left(2\pi f \cdot t\right)}{\left|\underline{I^?_{out}}\right| \cdot \sin\left(2\pi f \cdot t\right)} = \frac{10\ V}{26.542\ mA} = 376.76\ \Omega \tag{57}$$

4. Frequency Behaviour of the Circuit

In this section, we will focus on the frequency behaviour of the pnp-common-base transistor circuit in Figure 1. The main focus is the bode-diagram. For that, two different analysis concepts are presented. On the one hand, the analysis will be done via the conventional frequency response method, which will be shown in section 4.1 and on the other hand, the two-port analysis concept will be used (see section 4.2).

4.1. Conventional Method

This section represents why the small-signal parameters are that important. By using the small-signal parameters from section 3.2 to 3.8, a single-ended amplifier can be modelled, which is shown in Figure 13. The single-ended amplifier model is identical to the the small-signal equivalent circuit of the pnp-common-base transistor circuit. This ensures a simpler representation of the circuit. Moreover, the magnitude and phase response of the circuit can be calculated more easily.

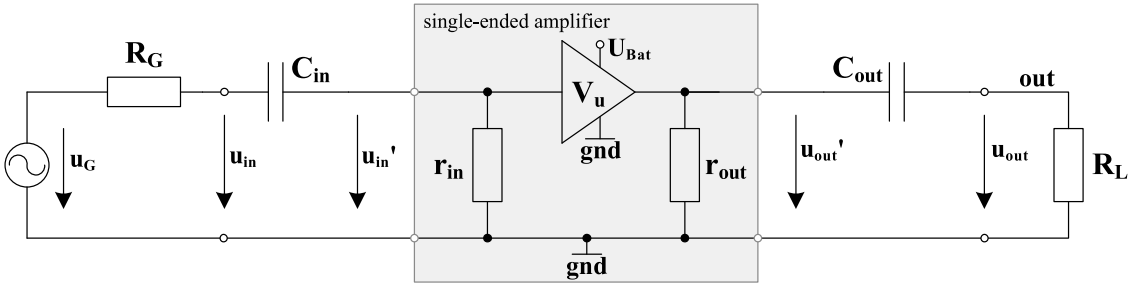

Figure 13: Common-base amplifier represented as single-ended amplifier

4.1.1. Calculation of the Magnitude and Phase Response

The input decoupling capacitor C_{in} forms a high-pass filter with the input terminal resistance r_{in} of the pnp-common-base transistor circuit (single-ended amplifier).

$$\underline{G_{in}}\,(j2\pi f) = \frac{\underline{U'_{in}}}{\underline{U_{in}}} = \frac{r_{in}}{\dfrac{1}{j2\pi f \cdot C_{in}} + r_{in}} \tag{58}$$

Due to the fact, that the used transistor model contains no energy storing devices, the frequency response is constant.

$$\underline{G_T}\,(j2\pi f) = \frac{\underline{U'_{out}}}{\underline{U'_{in}}} = V_u \tag{59}$$

Analogue to the input, the output decoupling capacitor C_{out} forms as well a high-pass filter with the output terminal resistance r_{out} of the pnp-common-base transistor circuit (single-ended amplifier).

$$\underline{G_{out}}\left(j2\pi f\right) = \frac{\underline{U_{out}}}{\underline{U'_{out}}} = \frac{R_L}{\frac{1}{j2\pi f \cdot C_{out}} + R_L} \tag{60}$$

By connecting all three frequency responses from equation 58 to 60, the overall frequency response can be represented as follows:

$$\underline{G}\left(j2\pi f\right) = \underline{G_{in}}\left(j2\pi f\right) \cdot \underline{G_T}\left(j2\pi f\right) \cdot \underline{G_{out}}\left(j2\pi f\right) \tag{61}$$

Furthermore, the magnitude response can be derived by taking the absolute value of the overall frequency response $\underline{G}\left(j2\pi f\right)$, which is shown in equation 61.

$$\left|\underline{G}\left(j2\pi f\right)\right|_{dB} = 20 \cdot \log_{10}\left|\frac{r_{in}}{\frac{1}{j2\pi f \cdot C_{in}} + r_{in}} \cdot V_u \cdot \frac{R_L}{\frac{1}{j2\pi f \cdot C_{out}} + R_L}\right| \tag{62}$$

Finally, the phase response can be derived by taking the argument of the overall frequency response $\underline{G}\left(j2\pi f\right)$, which is shown in equation 61.

$$arg\left(\underline{G}\left(j2\pi f\right)\right) = arg\left(\frac{r_{in}}{\frac{1}{j2\pi f \cdot C_{in}} + r_{in}} \cdot V_u \cdot \frac{R_L}{\frac{1}{j2\pi f \cdot C_{out}} + R_L}\right) \tag{63}$$

4.1.2. The Magnitude and Phase Response

Figure 14 below depicts the magnitude and phase response of the pnp-common-base transistor circuit with neglected parasitics. The graph is created from equation 62 and 63 which are visible on the previous page.

The slope of the magnitude response is not constant in the whole area of the transition-band[3]. This is due to the high-pass filters at the input and output terminal of the pnp-common-base transistor circuit. Each 1st order high-pass filter has it's own cut-off frequency. If those two cut-off frequency aren't equal (which is the case in the below depicted bode-plot), there will be a change in the slope at the transition-band region. Consequently, in the frequency range, where only one 1st order high-pass filter is present, there will be an attenuation of $-20dB/decade$. Whereas, in the frequency range, where two 1st order high-pass filter are present, there will be an attenuation of $-40dB/decade$.

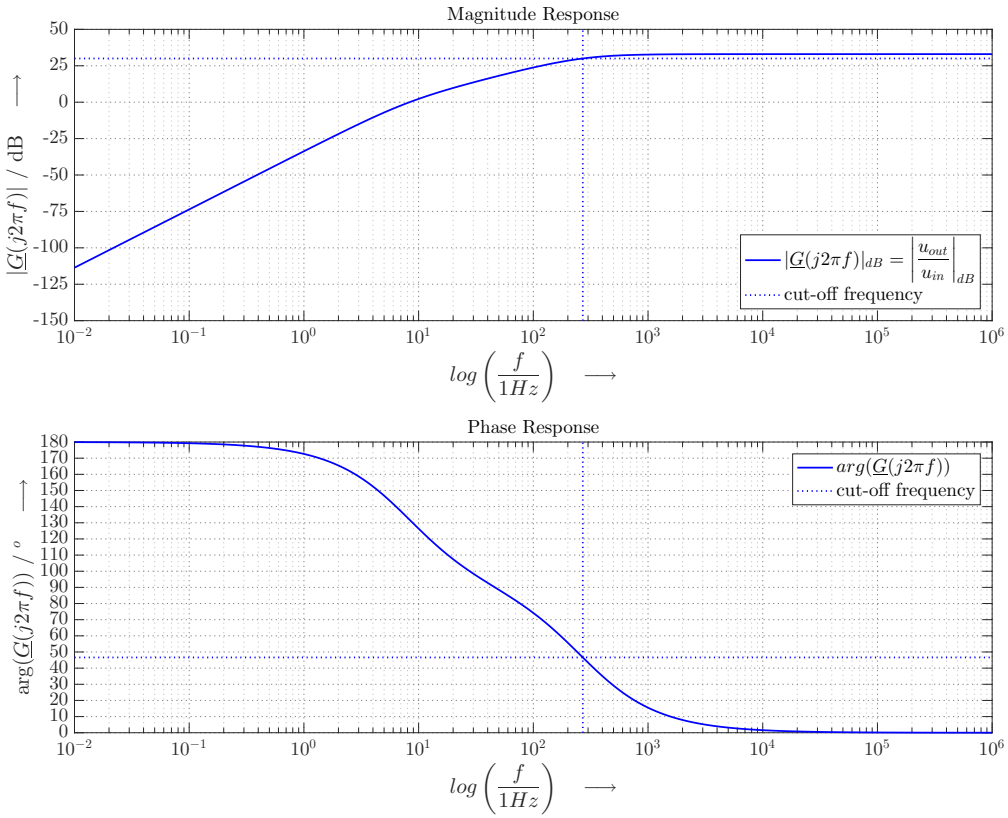

Figure 14: Magnitude and phase response of the single-ended amplifier

[3]The transition-band is a range of frequencies between the pass-band and the stop-band, where signals are transmitted, but damping is already present. The pass-band is a range of frequencies, where signals can pass through without any damping. The stop-band is a range of frequencies, where no signals are passing through.

4.2. Two-Port Theory for Circuit Analysis

Another possibility to determine the frequency response of the pnp-common-base transistor circuit, which is shown in Figure 1, is given by the two-port or quadrupole theory [11, p. 171]. Figure 15 and 16 below are representing the two main-topologies of the two-port theory. The goal is to disassemble the small-signal equivalent circuit from Figure 7 into parts of the two main-topologies.

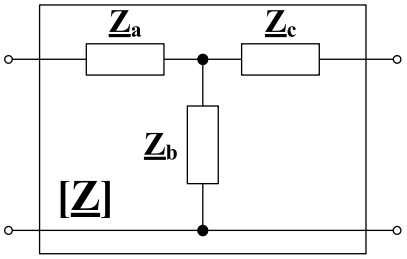

Figure 15: T-topology [3, p. 688]

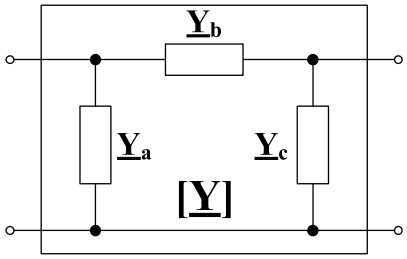

Figure 16: PI-topology [3, p. 688]

4.2.1. Important Two-Port Topologies and Characteristics

For analysing the circuit, three two-port matrices are used. The first one is the impedance characteristic [$\underline{\mathbf{Z}}$], where current is impressed at the terminals of the two-port, which leads to voltages at the input and output terminal of the two-port. The second characteristic is the admittance characteristic [$\underline{\mathbf{Y}}$], where voltages are applied at the terminals of the two-port. The result is a current flow in the input and output terminal. Finally, the third characteristic is called the chain characteristic [$\underline{\mathbf{A}}$], where the input voltage and current is defined by the output voltage and current.

T-Topology (Impedance Characteristic):

$$[\underline{\mathbf{Z}}] = \begin{bmatrix} \underline{Z}_{11} & \underline{Z}_{12} \\ \underline{Z}_{21} & \underline{Z}_{22} \end{bmatrix} = \begin{bmatrix} \underline{Z}_a + \underline{Z}_b & \underline{Z}_b \\ \underline{Z}_b & \underline{Z}_b + \underline{Z}_c \end{bmatrix} \quad \Rightarrow \quad \begin{bmatrix} \underline{U}_1 \\ \underline{U}_2 \end{bmatrix} = \begin{bmatrix} \underline{Z}_{11} & \underline{Z}_{12} \\ \underline{Z}_{21} & \underline{Z}_{22} \end{bmatrix} \cdot \begin{bmatrix} \underline{I}_1 \\ \underline{I}_2 \end{bmatrix} \tag{64}$$

PI-Topology (Admittance Characteristic):

$$[\underline{\mathbf{Y}}] = \begin{bmatrix} \underline{Y}_{11} & \underline{Y}_{12} \\ \underline{Y}_{21} & \underline{Y}_{22} \end{bmatrix} = \begin{bmatrix} \underline{Y}_a + \underline{Y}_b & -\underline{Y}_b \\ -\underline{Y}_b & \underline{Y}_b + \underline{Y}_c \end{bmatrix} \quad \Rightarrow \quad \begin{bmatrix} \underline{I}_1 \\ \underline{I}_2 \end{bmatrix} = \begin{bmatrix} \underline{Y}_{11} & \underline{Y}_{12} \\ \underline{Y}_{21} & \underline{Y}_{22} \end{bmatrix} \cdot \begin{bmatrix} \underline{U}_1 \\ \underline{U}_2 \end{bmatrix} \tag{65}$$

Chain Characteristic[4]:

$$[\underline{\mathbf{A}}] = \begin{bmatrix} \underline{A}_{11} & \underline{A}_{12} \\ \underline{A}_{21} & \underline{A}_{22} \end{bmatrix} \quad \Rightarrow \quad \begin{bmatrix} \underline{U}_1 \\ \underline{I}_1 \end{bmatrix} = \begin{bmatrix} \underline{A}_{11} & \underline{A}_{12} \\ \underline{A}_{21} & \underline{A}_{22} \end{bmatrix} \cdot \begin{bmatrix} \underline{U}_2 \\ \tilde{I}_2 \end{bmatrix} = \begin{bmatrix} \underline{A}_{11} & \underline{A}_{12} \\ \underline{A}_{21} & \underline{A}_{22} \end{bmatrix} \cdot \begin{bmatrix} \underline{U}_2 \\ -\underline{I}_2 \end{bmatrix} \tag{66}$$

[4]By definition, current counting arrows are pointing into the two-port. The Chain-Characteristic is conceived for connecting multiple blocks in a chain (one behind the other). For that reason the current $\underline{I}_2$ receives a negative sign.

4.2.2. Conversion Table and Two-Port Properties

Table 5 lists the conversion between different two-port matrices[5]. Each row represents a two-port matrix. If a conversion needs to be applied on a given matrix, we have to look to the row, where the matrix of interest is listed. First, we have to find the „1“, which represents a part of the multiplier in front of the matrix of interest. Next, we have to keep the column c_i, where the „1“ is depicted and go to the corresponding cell entry of the matrix, which needs to be converted. This cell entry is the denominator of the term which gets multiplied in front of the matrix of interest. Each cell of the matrix of interest is filled by the cell of the matrix to be converted, which is depicted in the corresponding column c_i.

Table 5: Conversion table between the different matrices [1, p. 873]

	c_1	c_2	c_3	c_4	c_5	c_6
$[\underline{\mathbf{Z}}]$	1	$\underline{Z}_{11}$	$\underline{Z}_{12}$	$\underline{Z}_{21}$	$\underline{Z}_{22}$	$\det[\underline{\mathbf{Z}}]$
$[\underline{\mathbf{Y}}]$	$\det[\underline{\mathbf{Y}}]$	$\underline{Y}_{22}$	$-\underline{Y}_{12}$	$-\underline{Y}_{21}$	$\underline{Y}_{11}$	1
$[\underline{\mathbf{A}}]$	$\underline{A}_{21}$	$\underline{A}_{11}$	$\det[\underline{\mathbf{A}}]$	1	$\underline{A}_{22}$	$\underline{A}_{12}$
$[\underline{\mathbf{B}}]$	$-\underline{B}_{21}$	$\underline{B}_{22}$	1	$\det[\underline{\mathbf{B}}]$	$\underline{B}_{11}$	$-\underline{B}_{12}$
$[\underline{\mathbf{H}}]$	$\underline{H}_{22}$	$\det[\underline{\mathbf{H}}]$	$\underline{H}_{12}$	$-\underline{H}_{21}$	1	$\underline{H}_{11}$
$[\underline{\mathbf{P}}]$	$\underline{P}_{11}$	1	$-\underline{P}_{12}$	$\underline{P}_{21}$	$\det[\underline{\mathbf{P}}]$	$\underline{P}_{22}$

4.2.3. Disassembled Small-Signal Equivalent Circuit

The small-signal equivalent circuit, shown in Figure 7, is disassembled into 4 parts after the signal source. Those parts are modelled as two-ports and are depicted below.

The two-port shown in Figure 17 represents the circuit which connects the transistor with the signal source.

$$\left[\underline{\mathbf{Z_E}}\right] = \begin{bmatrix} \frac{1}{j\omega C_{in}} + R_E & R_E \\ R_E & R_E \end{bmatrix} \tag{67}$$

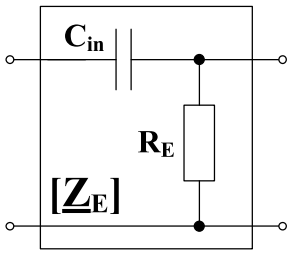

Figure 17: T-topology at emitter terminal

The two-port shown in Figure 18 represents the simplified small-signal transistor model of the pnp-common-base circuit. The derivation of the admittance characteristic is depicted on the next page.

$$\left[\underline{\mathbf{Y_T}}\right] = \begin{bmatrix} (B+1)\cdot g_{BE} + g_{CE} & -g_{CE} \\ -g_{CE} - g_{BE}\cdot B & g_{CE} \end{bmatrix} \tag{68}$$

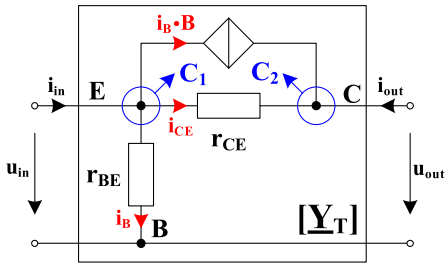

Figure 18: Simplified transistor model

[5]Style of the table arrangement comes from Ao.Univ.-Prof. Dipl.-Ing. Dr.techn. Magele Christian.

Derivation of the admittance characteristic of the transistor model:

The derivation below describes the behaviour of the two-port transistor model shown in Figure 18.

$$m: \; -u_{in} + u_{CE} + u_{out} = 0 \Leftrightarrow u_{CE} = u_{in} - u_{out}$$

$$\begin{aligned} C_1: \quad & -i_{in} + i_B + i_{CE} + i_B \cdot B = 0 \Leftrightarrow i_{in} = i_B \cdot (1+B) + i_{CE} \\ \Leftrightarrow \quad & i_{in} = \frac{u_{in}}{r_{BE}} \cdot (1+B) + \frac{u_{in} - u_{out}}{r_{CE}} = u_{in} \cdot \left(\frac{1+B}{r_{BE}} + \frac{1}{r_{CE}} \right) + u_{out} \cdot \left(-\frac{1}{r_{CE}} \right) \\ \Leftrightarrow \quad & i_{in} = u_{in} \cdot ((1+B) \cdot g_{BE} + g_{CE}) + u_{out} \cdot (-g_{CE}) \end{aligned}$$

$$\begin{aligned} C_2: \quad & -i_{out} - i_{CE} - i_B \cdot B = 0 \Leftrightarrow i_{out} = -i_{CE} - i_B \cdot B \\ \Leftrightarrow \quad & i_{out} = \frac{u_{out} - u_{in}}{r_{CE}} - \frac{u_{in}}{r_{BE}} \cdot B = u_{in} \cdot \left(-\frac{1}{r_{CE}} - \frac{1}{r_{BE}} \cdot B \right) + u_{out} \cdot \left(\frac{1}{r_{CE}} \right) \\ \Leftrightarrow \quad & i_{out} = u_{in} \cdot (-g_{CE} - g_{BE} \cdot B) + u_{out} \cdot (g_{CE}) \end{aligned}$$

$$\overset{(100)}{\Longrightarrow} \quad \begin{bmatrix} \underline{I_{in}} \\ \underline{I_{out}} \end{bmatrix} = \underbrace{\begin{bmatrix} (1+B) \cdot g_{BE} + g_{CE} & -g_{CE} \\ -g_{CE} - g_{BE} \cdot B & g_{CE} \end{bmatrix}}_{[\underline{\mathbf{Y_T}}]} \cdot \begin{bmatrix} \underline{U_{in}} \\ \underline{U_{out}} \end{bmatrix} \tag{69}$$

The two-port shown in Figure 19 represents the circuit which connects the transistor with the load.

$$\left[\underline{\mathbf{Y_C}}\right] = \begin{bmatrix} \frac{1}{R_C} + j\omega C_{out} & -j\omega C_{out} \\ -j\omega C_{out} & j\omega C_{out} \end{bmatrix} \tag{70}$$

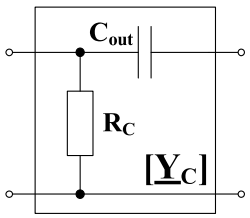

Figure 19: PI-topology at collector terminal

The tow-port shown in Figure 20 represents the load of the transistor circuit.

$$\left[\underline{\mathbf{Z_L}}\right] = \begin{bmatrix} R_L & R_L \\ R_L & R_L \end{bmatrix} \tag{71}$$

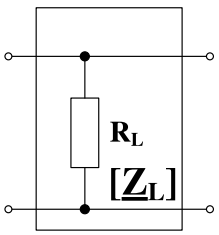

Figure 20: T-topology of the load

4.2.4. Matrix-Conversion for Chain-Characteristic Representation

To get the overall frequency behaviour of the circuit, all individual two-ports need to be connected in a row. This is only possible with the [$\underline{\mathbf{A}}$] matrix. First, all two-port matrices from the previous pages must be converted into a [$\underline{\mathbf{A}}$] matrix. For that, the conversion Table 5 from section 4.2.2 is used.

The chain-characteristic of the two-port, shown in Figure 17, can be expressed via the impedance parameters as follows:

$$\left[\underline{\mathbf{Z_E}}\right] = \begin{bmatrix} \underline{Z_{E}}_{11} & \underline{Z_{E}}_{12} \\ \underline{Z_{E}}_{21} & \underline{Z_{E}}_{22} \end{bmatrix} \quad \Leftrightarrow \quad \left[\underline{\mathbf{A_E}}\right] = \frac{1}{\underline{Z_{E}}_{21}} \cdot \begin{bmatrix} \underline{Z_{E}}_{11} & \det\left[\underline{\mathbf{Z_E}}\right] \\ 1 & \underline{Z_{E}}_{22} \end{bmatrix} = \begin{bmatrix} \underline{A_{E}}_{11} & \underline{A_{E}}_{12} \\ \underline{A_{E}}_{21} & \underline{A_{E}}_{22} \end{bmatrix} \tag{72}$$

After plugging in the cell contents of equation 67, the chain-characteristic is given by:

$$\left[\underline{\mathbf{A_E}}\right] = \frac{1}{R_E} \cdot \begin{bmatrix} \frac{1}{j\omega C_{in}} + R_E & \frac{R_E}{j\omega C_{in}} \\ 1 & R_E \end{bmatrix} \tag{73}$$

The chain-characteristic of the two-port, shown in Figure 18, can be expressed via the admittance parameters as follows:

$$\left[\underline{\mathbf{Y_T}}\right] = \begin{bmatrix} \underline{Y_{T}}_{11} & \underline{Y_{T}}_{12} \\ \underline{Y_{T}}_{21} & \underline{Y_{T}}_{22} \end{bmatrix} \quad \Leftrightarrow \quad \left[\underline{\mathbf{A_T}}\right] = \frac{-1}{\underline{Y_{T}}_{21}} \cdot \begin{bmatrix} \underline{Y_{T}}_{22} & 1 \\ \det\left[\underline{\mathbf{Y_T}}\right] & \underline{Y_{T}}_{11} \end{bmatrix} = \begin{bmatrix} \underline{A_{T}}_{11} & \underline{A_{T}}_{12} \\ \underline{A_{T}}_{21} & \underline{A_{T}}_{22} \end{bmatrix} \tag{74}$$

After plugging in the cell contents of equation 68, the chain-characteristic is given by:

$$\left[\underline{\mathbf{A_T}}\right] = \frac{1}{g_{CE} + g_{BE} \cdot B} \cdot \begin{bmatrix} g_{CE} & 1 \\ g_{BE} \cdot g_{CE} & (B+1) \cdot g_{BE} + g_{CE} \end{bmatrix} \tag{75}$$

The chain-characteristic of the two-port, shown in Figure 19, can be expressed via the admittance parameters as follows:

$$\left[\underline{\mathbf{Y_C}}\right] = \begin{bmatrix} \underline{Y_{C}}_{11} & \underline{Y_{C}}_{12} \\ \underline{Y_{C}}_{21} & \underline{Y_{C}}_{22} \end{bmatrix} \quad \Leftrightarrow \quad \left[\underline{\mathbf{A_C}}\right] = \frac{-1}{\underline{Y_{C}}_{21}} \cdot \begin{bmatrix} \underline{Y_{C}}_{22} & 1 \\ \det\left[\underline{\mathbf{Y_C}}\right] & \underline{Y_{C}}_{11} \end{bmatrix} = \begin{bmatrix} \underline{A_{C}}_{11} & \underline{A_{C}}_{12} \\ \underline{A_{C}}_{21} & \underline{A_{C}}_{22} \end{bmatrix} \tag{76}$$

After plugging in the cell contents of equation 70, the chain-characteristic is given by:

$$\left[\underline{\mathbf{A_C}}\right] = \frac{1}{j\omega C_{out}} \cdot \begin{bmatrix} j\omega C_{out} & 1 \\ \frac{j\omega C_{out}}{R_C} & \frac{1}{R_C} + j\omega C_{out} \end{bmatrix} \tag{77}$$

The chain-characteristic of the two-port, shown in Figure 20, can be expressed via the impedance parameters as follows:

$$\left[\underline{\mathbf{Z_L}}\right] = \begin{bmatrix} \underline{Z_{L}}_{11} & \underline{Z_{L}}_{12} \\ \underline{Z_{L}}_{21} & \underline{Z_{L}}_{22} \end{bmatrix} \quad \Leftrightarrow \quad \left[\underline{\mathbf{A_L}}\right] = \frac{1}{\underline{Z_{L}}_{21}} \cdot \begin{bmatrix} \underline{Z_{L}}_{11} & \det\left[\underline{\mathbf{Z_L}}\right] \\ 1 & \underline{Z_{L}}_{22} \end{bmatrix} = \begin{bmatrix} \underline{A_{L}}_{11} & \underline{A_{L}}_{12} \\ \underline{A_{L}}_{21} & \underline{A_{L}}_{22} \end{bmatrix} \tag{78}$$

After plugging in the cell contents of equation 71, the chain-characteristic is given by:

$$\left[\underline{\mathbf{A_L}}\right] = \frac{1}{R_L} \cdot \begin{bmatrix} R_L & 0 \\ 1 & R_L \end{bmatrix} \tag{79}$$

4.2.5. Input Terminal Impedance

With the knowledge of the chain characteristics from section 4.2.4, the input terminal impedance $\underline{Z_{in}}$, which the source sees at their clamps, can be determined. To perform this calculation, the two-port matrices $\left[\underline{\mathbf{A_E}}\right]$, $\left[\underline{\mathbf{A_T}}\right]$ and $\left[\underline{\mathbf{A_C}}\right]$ are connected together, which is shown in Figure 21 below.

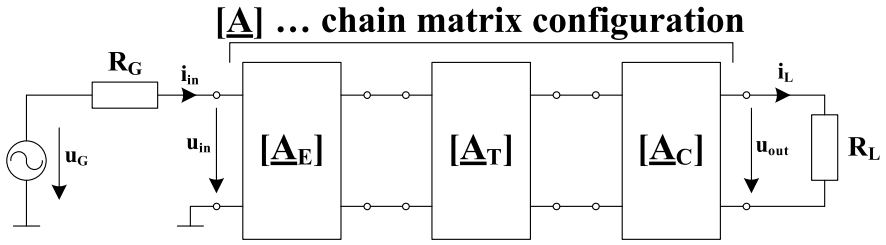

Figure 21: Circuit for calculating the input-impedance $\underline{Z_{in}}$

Next, a matrix multiplication is applied to get a single admittance matrix $[\underline{\mathbf{A}}]$, which can be easily converted back to an impedance matrix $[\underline{\mathbf{Z}}]$. Moreover, with the impedance matrix $[\underline{\mathbf{Z}}]$, the input-impedance $\underline{Z_{in}}$, which the source sees, can be calculated.

$$[\underline{\mathbf{A}}] = \left[\underline{\mathbf{A_E}}\right] \cdot \left[\underline{\mathbf{A_T}}\right] \cdot \left[\underline{\mathbf{A_C}}\right] \quad \Leftrightarrow \quad [\underline{\mathbf{Z}}] = \frac{1}{\underline{A}_{21}} \cdot \begin{bmatrix} \underline{A}_{11} & \det[\underline{\mathbf{A}}] \\ 1 & \underline{A}_{22} \end{bmatrix} = \begin{bmatrix} \underline{Z}_{11} & \underline{Z}_{12} \\ \underline{Z}_{21} & \underline{Z}_{22} \end{bmatrix} \tag{80}$$

With the impedance matrix $[\underline{\mathbf{Z}}]$ from equation 80 we are able to determine the input impedance $\underline{Z_{in}}$. The circuit for calculating the input impedance $\underline{Z_{in}}$ is depicted in Figure 22 and 23 below.

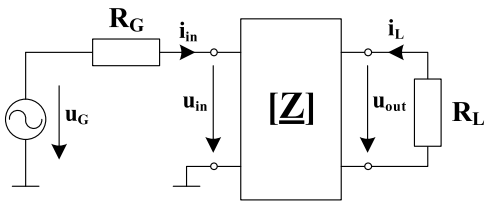

Figure 22: Impedance matrix between source and load

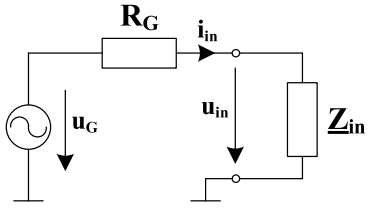

Figure 23: Source connected to input-impedance model

Derivation of the Input Terminal Impedance:

The derivation below describes the input terminal impedance $\underline{Z}_{in}$ depending on a given frequency of the pnp-common-base transistor circuit, which is shown in Figure 1.

$$\begin{bmatrix} \underline{U}_{in} \\ \underline{U}_{out} \end{bmatrix} = \begin{bmatrix} \underline{Z}_{11} & \underline{Z}_{12} \\ \underline{Z}_{21} & \underline{Z}_{22} \end{bmatrix} \cdot \begin{bmatrix} \underline{I}_{in} \\ \underline{I}_{L} \end{bmatrix} \quad \Rightarrow \quad \begin{cases} \text{I:} & \underline{U}_{in} = \underline{Z}_{11} \cdot \underline{I}_{in} + \underline{Z}_{12} \cdot \underline{I}_{L} \\ \text{II:} & \underline{U}_{out} = \underline{Z}_{21} \cdot \underline{I}_{in} + \underline{Z}_{22} \cdot \underline{I}_{L} \end{cases}$$

$$\Rightarrow \quad \text{II: } \underline{U}_{out} = \underline{Z}_{21} \cdot \underline{I}_{in} + \underline{Z}_{22} \cdot \underline{I}_{L} \stackrel{!}{=} -R_L \cdot \underline{I}_{L} \quad \Leftrightarrow \quad \underline{I}_{L} = -\frac{\underline{Z}_{21}}{(\underline{Z}_{22} + R_L)} \cdot \underline{I}_{in}$$

$$\Rightarrow \quad \text{I: } \underline{U}_{in} = \underline{Z}_{11} \cdot \underline{I}_{in} + \underline{Z}_{12} \cdot \underline{I}_{L} = \underline{Z}_{11} \cdot \underline{I}_{in} - \frac{\underline{Z}_{21}}{(\underline{Z}_{22} + R_L)} \cdot \underline{I}_{in}$$

$$\Leftrightarrow \quad \text{I: } \underline{U}_{in} = \frac{\overbrace{\underline{Z}_{11} \cdot \underline{Z}_{22} - \underline{Z}_{12} \cdot \underline{Z}_{21}}^{\det[\underline{\mathbf{Z}}]} - R_L \cdot \underline{Z}_{11}}{\underline{Z}_{22} + R_L} \cdot \underline{I}_{in}$$

$$\Leftrightarrow \quad \text{I: } \underline{U}_{in} = \frac{\det\left[\underline{\mathbf{Z}}\right] - R_L \cdot \underline{Z}_{11}}{\underline{Z}_{22} + R_L} \cdot \underline{I}_{in}$$

$$\Leftrightarrow \quad \text{I: } \underline{Z}_{in} = \frac{\underline{U}_{in}}{\underline{I}_{in}} = \frac{\det\left[\underline{\mathbf{Z}}\right] - R_L \cdot \underline{Z}_{11}}{\underline{Z}_{22} + R_L} \tag{81}$$

In Figure 24 below is the frequency behaviour of the input terminal impedance $\underline{Z}_{in}$ depicted. The graph is created out of equation 81, where the frequency is increased from 1 Hz towards 1 kHz. It is visible that for low frequencies the input terminal impedance $\underline{Z}_{in}$ is high. This is due to the high-pass filter at the input and output terminal of the circuit. The dominant filter is the high-pass filter at the input terminal, because the terminal input resistance r_{in} is much lower than the load resistance R_L. This causes a higher cut-off frequency, which limits the amplifier bandwidth.

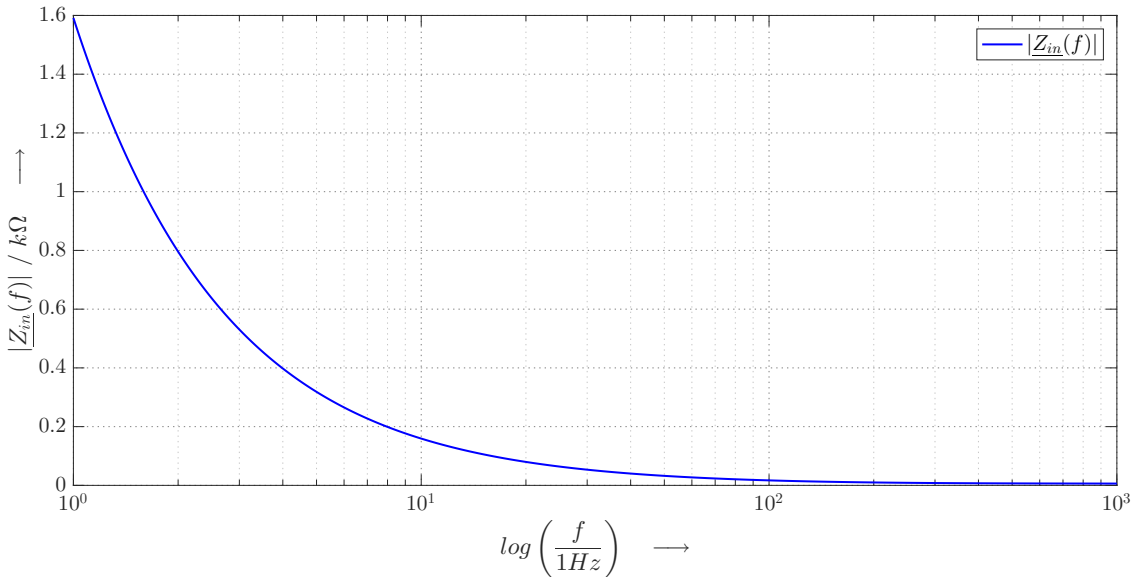

Figure 24: Input-terminal impedance over frequency

4.2.6. Calculation of the Magnitude and Phase Response

With the knowledge of the chain characteristics from section 4.2.4, the overall chain matrix $\left[\underline{\mathbf{A_O}}\right]$ can be determined. To perform this calculation, the two-port matrices $\left[\underline{\mathbf{A_E}}\right]$, $\left[\underline{\mathbf{A_T}}\right]$, $\left[\underline{\mathbf{A_C}}\right]$ and $\left[\underline{\mathbf{A_L}}\right]$ are connected together, which is shown in Figure 25 below.

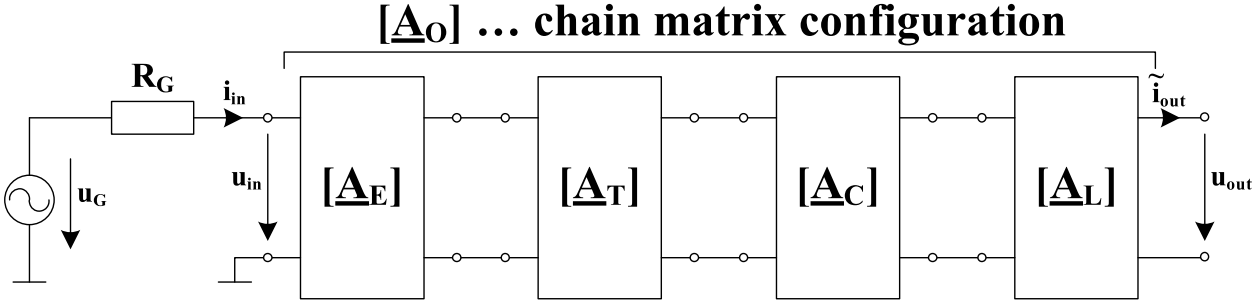

Figure 25: Circuit for frequency response determination

Next, a matrix multiplication is applied to get the overall chain matrix $\left[\underline{\mathbf{A_O}}\right]$. Moreover, out of the overall chain matrix $\left[\underline{\mathbf{A_O}}\right]$, the frequency response $\underline{H}\left(j\omega\right)$, which corresponds to the reciprocal value of the first pivot element $\underline{A_{O}}_{11}$ in the chain matrix, can be determined.

$$\left[\underline{\mathbf{A_O}}\right] = \left[\underline{\mathbf{A_E}}\right] \cdot \left[\underline{\mathbf{A_T}}\right] \cdot \left[\underline{\mathbf{A_C}}\right] \cdot \left[\underline{\mathbf{A_L}}\right] = \begin{bmatrix} \underline{A_{O}}_{11} & \underline{A_{O}}_{12} \\ \underline{A_{O}}_{21} & \underline{A_{O}}_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{\underline{H}} & \underline{A_{O}}_{12} \\ \underline{A_{O}}_{21} & \underline{A_{O}}_{22} \end{bmatrix} \tag{82}$$

By taking the reciprocal value of the first pivot element $\underline{A_{O}}_{11}$ of the overall chain matrix $\left[\underline{\mathbf{A_O}}\right]$ from equation 82, the expression for the frequency response $\underline{H}\left(j\omega\right)$ appears.

$$\underline{H}\left(j\omega\right) = \frac{1}{\underline{A_{O}}_{11}} \tag{83}$$

Furthermore, the magnitude response can be derived by taking the absolute value of the overall frequency response $\underline{H}\left(j\omega\right)$, which is shown equation 83.

$$\left|\underline{H}\left(j2\pi f\right)\right|_{dB} = \left|\underline{H}\left(j\omega\right)\right|_{dB} = 20 \cdot \log_{10}\left|\underline{H}\left(j\omega\right)\right| = 20 \cdot \log_{10}\left|\frac{1}{\underline{A_{O}}_{11}}\right| \tag{84}$$

Finally, the phase response can be derived by taking the argument of the overall frequency response $\underline{H}\left(j\omega\right)$, which is shown equation 83.

$$arg\left(\underline{H}\left(j2\pi f\right)\right) = arg\left(\underline{H}\left(j\omega\right)\right) = arg\left(\underline{H}\left(j\omega\right)\right) = arg\left(\frac{1}{\underline{A_{O}}_{11}}\right) \tag{85}$$

In Figure 26 below is the magnitude and phase response of the pnp-common-base transistor circuit depicted. The plot is generated out of equation 84 and 85, where the frequency is increased from 10 mHz towards 1 MHz. It is visible that the circuit stays for low frequencies in the transition-band. In that region the circuit has a non-constant amplification. For very low frequencies the amplification will disappear and the attenuation will appear. This is due to the high-pass filter at the input and output terminal of the circuit. The dominant filter is the high-pass filter at the input terminal, because the terminal input resistance r_{in} is much lower than the load resistance R_L. This causes a higher cut-off frequency, which limits the amplifier bandwidth.

The two cut-off frequencies, which are basically the cut-off frequencies of first-order high-pass filters, are depicted in equation 86 and 87 below [3, p. 533].

$$f_{c_{in}} = \frac{1}{2\pi \cdot r_{in} \cdot C_{in}} = 269.47\ Hz \qquad (86) \qquad f_{c_{out}} = \frac{1}{2\pi \cdot R_L \cdot C_{out}} = 7.96\ Hz \qquad (87)$$

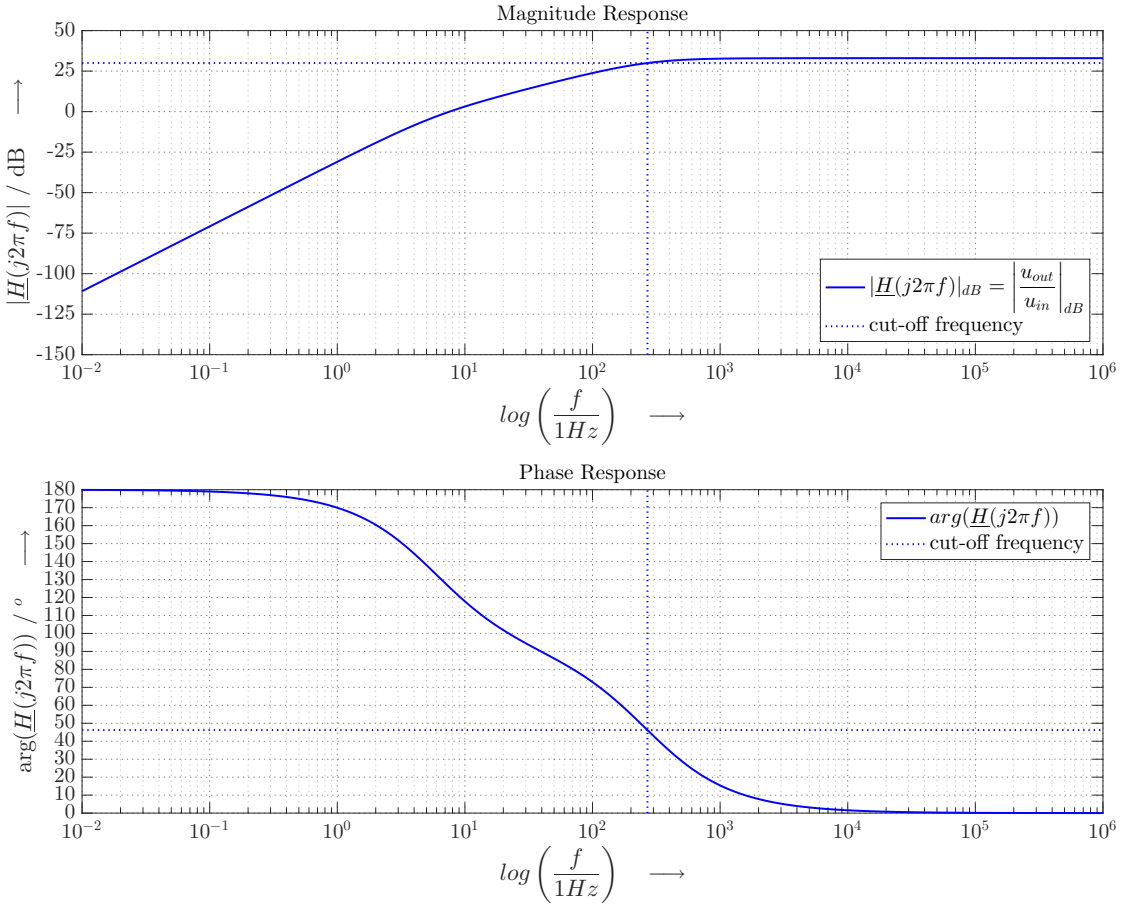

Figure 26: Magnitude and phase response of the two-port model

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List of Symbols

Symbol	*Description*	*Page*
R_G[6]	internal resistance of the waveform generator	1
R_1	resistor for defining the base bias voltage	1
R_2	resistor for defining the base bias voltage	1
R_E	emitter resistor	1
R_C	collector resistor	1
R_L	load resistor	1
C_B	base capacitor	1
C_{in}	input filter capacitor	1
C_{out}	output filter capacitor	1
Q	transistor	1
U_{Egnd}	emitter voltage with respect to ground	1
U_{R1}	voltage drop over R_1	1
U_{R2}	voltage drop over R_2	1
U_{Bat}	supply voltage - Bat is an acronym for battery	1
U_{BE}	base-emitter voltage	1
U_{CE}	collector-emitter voltage	1
U_{RE}	voltage drop over R_E	1
U_{RC}	voltage drop over R_C	1
I_{R1}	current through R_1	1
I_{R2}	current through R_2	1
I_B	base current	1
I_C	collector current	1
I_E	emitter current	1
I_{RE}	current through R_E	1
I_{RC}	current through R_C	1

[6] capital letters are depicting time independent values

Symbol	***Description***	***Page***
u_G[7]	waveform generator voltage	1
u_{in}	input voltage of the circuit	1
u_{out}	output voltage of the circuit	1
i_{in}	input current of the circuit	1
i_{out}	output current of the circuit	1
m_i	green/black m's are depicting voltage meshes	1
C_i	blue/black C's are depicting cut-sets or rather current nodes	1
U_{CEsat}	collector-emitter saturation voltage - voltage before reaching the saturation region of the transistor	2
U_{EA}	early-voltage	2
$B = h_{FE}$	large-signal or DC current gain	2
T	temperature	2
I_D	diode forward current	3
U_D	diode forward voltage	3
U_T	temperature voltage	3
k	Boltzmann-Constant $k = 1.38064852 \cdot 10^{-23}\ {}^{J}/_{K}$	3
q	elementary charge $q = 1.602176634 \cdot 10^{-19}\ C$	3
I_S	saturation reverse current	3
I_T	current being transported completely across the base region of the transistor	4
g_m	transconductance	9
i_C	small-signal collector current	8
u_{BE}	small-signal base-emitter voltage	8
$\beta = h_{fe}$	small-signal current gain	8
i_B	small-signal base current	8
r_{BE}	small-signal or rather differential base-emitter resistance	10
r_{CE}	small-signal or rather differential collector-emitter resistance	11
g_{CE}	small-signal or rather differential collector-emitter conductance	11

[7] lower case letters are depicting time dependent values

Symbol	***Description***	***Page***
u_{CE}	small-signal collector-emitter voltage	11
V_u	small-signal voltage gain	12
r_{in}	input terminal resistance	13
i_{RE}	small-signal current through the emitter-resistor R_E	13
i_{CE}	small-signal collector-emitter current - current through the differential collector-emitter resistance	13
i_{RC}	small-signal current through the collector-resistor R_C	13
r_{out}	output terminal resistance	13
α	wildcard - substitutes unwiedly expression	15
δ	wildcard - substitutes unwiedly expression	15
ϵ	wildcard - substitutes unwiedly expression	16
γ	wildcard - substitutes unwiedly expression	16
CS_i	side condition	17
$i_{in}^?$	unknown input current from ideal independent voltage source u_{in}	18
u_{ni}	node-voltages	18
$i_B^?$	unknown base current for controlling the dependent source	18
$i_C^?$	unknown collector current from dependent current source	18
G_E	emitter conductance - reciprocal of R_E	18
G_C	collector conductance - reciprocal of R_C	18
g_{BE}	base-emitter conductance - reciprocal of g_{BE}	18
G_L	load conductance - reciprocal of R_L	18
$\underline{U_{in}}$	input voltage phasor	20
$\underline{I_{in}}^?$	unknown input current phasor from ideal independent voltage source $\underline{U_{in}}$	20
$\underline{I_C}^?$	unknown collector current phasor from dependent current source	20
$\underline{I_B}^?$	unknown base current phasor for controlling the dependent source	20
$\hat{U}_{in}$	peak value of the input voltage	20
$\underline{u_{in}}(t)$	complex time dependent input voltage	20
$\underline{\mathbf{Y}}$	admittance matrix of the node-voltage method	20

Symbol	***Description***	***Page***
$\vec{S}$	source vector of the node-voltage method	20
$i_{out}^{?}$	unknown output current from ideal independent voltage source u_{out}	21
G_G	internal conductance of the waveform generator - reciprocal of R_G	23
$\underline{U_{out}}$	output voltage phasor	23
$\underline{i_{out}}^{?}$	unknown output current phasor from ideal independent voltage source $\underline{U_{out}}$	23
$\hat{U}_{out}$	peak value of the output voltage	23
$\underline{u_{out}}\,(t)$	complex time dependent output voltage	23
u'_{in}	input voltage to be amplified	24
u'_{out}	open-loop output voltage	24
$\underline{u_{in}}'$	input voltage phasor to be amplified	24
$\underline{u_{out}}'$	open-loop output voltage phasor	24
$\underline{G_{in}}\,(j2\pi f)$	frequency response of the input-sided high-pass filter	24
$\underline{G_T}\,(j2\pi f)$	frequency response of the intrinsic amplifier circuit	24
$\underline{G_{out}}\,(j2\pi f)$	frequency response of the output-sided high-pass filter	25
$\underline{G}\,(j2\pi f)$	overall frequency response of the pnp-common-base amplifier	25
$\underline{Z_a}$	input-sided longitudinal impedance of the T-Topology	27
$\underline{Z_b}$	shunt impedance of the T-Topology	27
$\underline{Z_c}$	output-sided longitudinal impedance of the T-Topology	27
$\underline{Y_a}$	input-sided shunt admittance of the PI-Topology	27
$\underline{Y_b}$	longitudinal admittance of the PI-Topology	27
$\underline{Y_c}$	output-sided shunt admittance of the PI-Topology	27
$\left[\underline{\mathbf{Z_i}}\right]$	impedance matrix	27
$\underline{Z_{ij}}$	impedance matrix element or cell	27
$\left[\underline{\mathbf{Y_i}}\right]$	admittance matrix	27
$\underline{Y_{ij}}$	admittance matrix element or cell	27
$\left[\underline{\mathbf{A_i}}\right]$	chain matrix	27
$\underline{A_{ij}}$	chain matrix element or cell	27

Symbol	***Description***	***Page***
$\left[\underline{\mathbf{B_i}}\right]$	inverse chain matrix	28
$\underline{B}_{ij}$	inverse chain matrix element or cell	28
$\left[\underline{\mathbf{H_i}}\right]$	hybrid matrix	28
$\underline{H}_{ij}$	hybrid matrix element or cell	28
$\left[\underline{\mathbf{P_i}}\right]$	inverse hybrid matrix	28
$\underline{P}_{ij}$	inverse hybrid matrix element or cell	28
$\underline{Z}_{in}$	input terminal impedance	31
$\underline{H}\,(j2\pi f)$	overall frequency response of the pnp-common-base amplifier	33
$f_{c_{in}}$	cut-off frequency of the input-sided high-pass filter	34
$f_{c_{out}}$	cut-off frequency of the output-sided high-pass filter	34
η	Eta-Factor - Factor which highlights the impact of the Early-Effect between U_{BE} and U_{CE}	43
VAF	forward Early-Voltage	43
h_{oe}	hybrid-parameter - output admittance	44
U_{EC}	emitter-collector voltage	45
$\underline{U}_{PQ}$	voltage between two nodes	48
$\underline{Z}_{PQ}$	impedance between two nodes	48
$\underline{I}_P$	node current	48
$\underline{I}_Q$	node current	48
$\underline{U}_P$	node voltage	48
$\underline{U}_Q$	node voltage	48
$\underline{Z}_P$	node to ground impedance	48
$\underline{Z}_Q$	node to ground impedance	48
A_v	voltage gain	48
C_F	feedback capacitor	48
C_{jCS}	collector to substrate junction capacitance	49
C_{jBC}	base to collector junction capacitance	49
C_{jBE}	base to emitter junction capacitance	49

Symbol	***Description***	***Page***
$u = u\,(t)$	time dependent voltage	58
$i = i\,(t)$	time dependent current	58
t	time parameters	58
$\hat{U}$	voltage peak value	58
ω	angular frequency	58
φ_u	initial voltage phase	58
$\underline{u}\,(t)$	complex time dependent voltage	58
$\underline{U}$	voltage phasor	58
$\hat{I}$	current peak value	58
φ_i	initial current phase	58
$\underline{i}\,(t)$	complex time dependent current	58
$\underline{I}$	current phasor	58

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A. Early-Effect and Early-Voltage Determination

In this section we will discuss the Early-Effect and the corresponding Early-Voltage U_{EA}. The Early-Voltage plays an important rule for calculating the small-signal parameters. Therefore, we have to find a way to determine the Early-Voltage.

A.1. Early-Effect

The **Early-Effect** is a second order effect, which translates to a **nonideality** in the device that can limit the gain of amplifiers [5, p. 145]. The result of the Early-Effect is a variation of the collector current I_C by changing the collector-emitter voltage U_{CE} in the active region of the BJT.

U_{BE} (at constant I_C) varies slightly with changing U_{CE}. This effect is caused by the variation of the effective base width W_B as U_{CE} changes, and it is given, approximately, by

$$\Delta U_{BE} = -\eta \cdot \Delta U_{CE}, \tag{88}$$

where $\eta = \frac{U_T}{U_{EA}+U_{CE}} \approx \frac{U_T}{U_{EA}} \approx 10^{-4} - 10^{-5}$ [12, p. 92]

.
According to [12, p. 93], the Early-Effect ...

- determines a transistor's collector-emitter resistance $r_{CE} = \frac{U_{EA}+U_{CE}}{I_C}$.
- sets a limit on single-stage voltage gain.

A.2. Early-Voltage Determination

Undoubtedly, there are several possibilities to get the Early-Voltage U_{EA}. The easiest way of getting the Early-Voltage of the used BJT is by searching through the corresponding ***SPICE*** model. The Early-Voltage U_{EA} is defined by the variable named VAF (e.g. $VAF = 21.11$), shown in listing 1 below.

Listing 1: BJT BC557B - Spice Model [13]

```
1  *Website Philips 23-02-00
2  *
3  .MODEL QBC557B PNP(
4  + IS=3.834E-14 NF=1.008 ISE=1.219E-14 NE=1.528 BF=344.4 IKF=0.08039
5  + VAF=21.11 NR=1.005 ISC=2.852E-13 NC=1.28 BR=14.84 IKR=0.047
6  + VAR=32.02 RB=1 IRB=1E-06 RBM=1 RE=0.6202 RC=0.5713
7  + XTB=0 EG=1.11 XTI=3 CJE=1.23E-11 VJE=0.6106 MJE=0.378
8  + TF=5.595E-10 XTF=3.414 VTF=5.23 ITF=0.1483 PTF=0 CJC=1.084E-11
9  + VJC=0.1022 MJC=0.3563 XCJC=0.6288 TR=1E-32 CJS=0 VJS=0.75
10 + MJS=0.333 FC=0.8027 )
11 *
```

Furthermore, the Early-Voltage can be determined by using the output characteristic of the BJT. An exemplary output characteristic is shown in Figure 27 below. Bear in mind that the slope of the curves in the linear operating region corresponds to the reciprocal value of the collector-emitter resistance r_{CE} of the respective operating point. It is visible that all curves intersect at one specific point of the U_{CE}-axis. This point represents the Early-Voltage U_{EA}. The output characteristic shows that for each curve, which is dependent on the base-current I_B, a different slope exists.

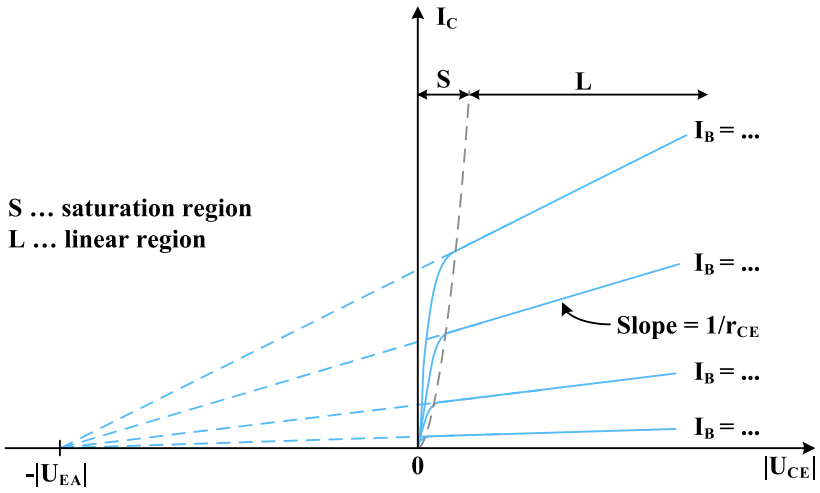

Figure 27: General output characteristic [4, p. 297]

With the output characteristic, we have two possibilities to calculate the Early-Voltage. First, the output admittance g_{CE}, which is given by the hybrid-parameter $h_{oe} = 60\ \mu S$ in the datasheet [14], and the corresponding collector current $I_C = 2\ mA$ and collector-emitter voltage $U_{CE} = -5\ V$ of the datasheet [14], the Early-Voltage can be calculated by the usage of the pnp equation 27.

$$\frac{1}{g_{CE}} = \frac{1}{h_{oe}} = -\frac{U_{CE} + U_{EA}}{I_C} \quad \Leftrightarrow \quad U_{EA} = -\frac{I_C}{h_{oe}} - U_{CE} = -\frac{2\ mA}{60\ \mu S} - (-5\ V) = -28.33\ V \tag{89}$$

Due to the fact that only the maximum output admittance g_{CE} or hybrid-parameter h_{oe} is given in the datasheet [14], it tends to be not accurate. That's why we have to come up with another concept for calculating the Early-Voltage U_{EA} in a more accurate way.

Generally speaking, the Early-Voltage U_{EA} can be determined by plotting the output characteristic of the BJT. Therefore a defined base current I_B is set, which is shown in Figure 28. Furthermore, the emitter-collector voltage U_{EC} is increased towards the absolute maximum ratings of the datasheet [14].

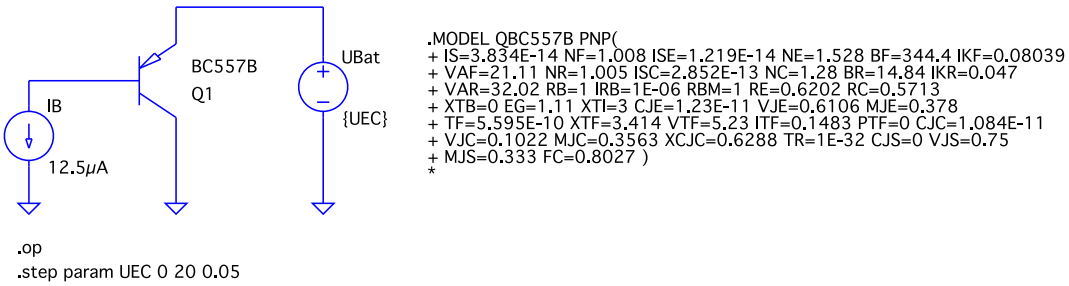

Figure 28: Circuit for Early-Voltage measurement

To generate the output characteristic, which is shown in Figure 29 below, the collector current I_C (flowing to ground - positive sign) and the collector-emitter voltage U_{CE}, which is the inverse of the emitter-collector voltage U_{EC}, gets recorded. The Early-Voltage U_{EA} can be determined by extrapolating the linear region of the output characteristic. The point where the extrapolation intersects with the U_{CE}-axis describes the absolute value of the Early-Voltage.

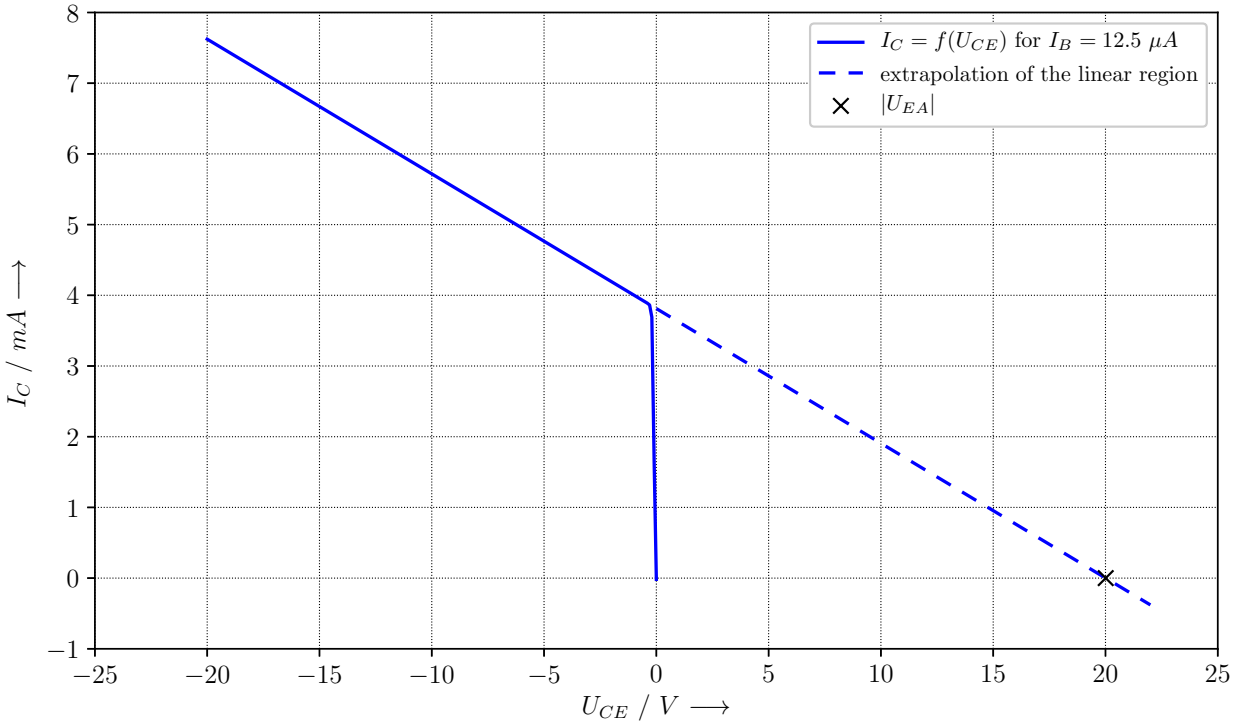

Figure 29: Output characteristic with corresponding Early-Voltage extrapolation

To get the extrapolation and subsequently the Early-Voltage U_{EA}, the parameters of of a linear equation have to be calculated. First, the slope of the linear region gets calculated, which is shown in equation 90 below. The negative sign of g_{CE} is related to the current and voltage counting-arrows. The counting-arrows of I_C and U_{CE} are not pointing in the same direction (see Figure 4).

$$-g_{CE} = \frac{I_{C_2} - I_{C_1}}{U_{CE_2} - U_{CE_1}} = \frac{7.242\ mA - 7.623\ mA}{-18\ V - (-20\ V)} = -190.5\ \mu S \tag{90}$$

Next, the collector saturation current $I_{C_{sat}}$ can be determined via the following equation.

$$I_{C_{sat}} = I_{C_1} + g_{CE} \cdot U_{CE_1} = 7.623\ mA + 190.5\ \mu S \cdot (-20\ V) = 3.813\ mA \tag{91}$$

With the knowledge of the above calculated parameters, the below depicted linear equation is well defined.

$$I_C = -g_{CE} \cdot U_{CE} + I_{C_{sat}} \tag{92}$$

Finally, the Early-Voltage is the point where the extrapolation intersects with the U_{CE}-axis. Due to that fact, the Early-Voltage U_{EA} can be determined via equation 92 and setting the collector current I_C to zero.

$$0 = -g_{CE} \cdot U_{CE}|_{EA} + I_{C_{sat}} \quad \Leftrightarrow \quad U_{EA} = -\,U_{CE}|_{EA} = -\frac{I_{C_{sat}}}{g_{CE}} = \frac{3.813\ mA}{190.5\ \mu S} = -20.02\ V \tag{93}$$

B. Miller's Theorem, Miller-Effect and Multiplication

So far we have discussed only the low frequency behaviour of the pnp-common-base transistor circuit. But what happens if the circuit reaches the high-frequency domain? For the high-frequency domain an important effect, named the Miller-Effect, appears. Actually, the Miller-Effect is present for all frequencies. But for inverting amplifiers, the input impedance decreases. This means that a capacitance appears increased at the input. This increased capacitance causes problems for high-frequency circuits.

B.1. Miller's Theorem

Miller's Theorem is an important tool for analysing the frequency response of a circuit just by inspection[8]. Miller says that floating impedances can be decomposed by two grounded impedances, which is shown in Figure 30 below.

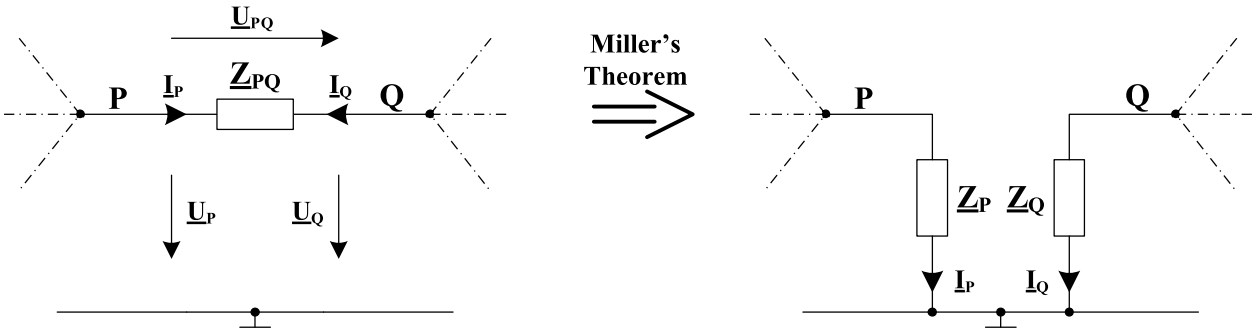

Figure 30: Miller's Theorem [5, p. 511]

To ensure that a floating impedance can be transformed into two grounded impedances, which is shown in Figure 30 above, the circuit must see the same load at node P and Q. Due to that fact the currents which are drawn in/out from node P and Q must stay the same.

$$\underline{I}_P = -\underline{I}_Q = \frac{\underline{U}_P - \underline{U}_Q}{\underline{Z}_{PQ}} \stackrel{!}{=} \frac{\underline{U}_P}{\underline{Z}_P} = -\frac{\underline{U}_Q}{\underline{Z}_Q} \tag{94}$$

With the above depicted equation 94, an expression for the grounded impedances $\underline{Z}_P$ and $\underline{Z}_Q$ can be derived by rearranging the equilibrium.

$$\underline{I}_P = \frac{\underline{U}_P - \underline{U}_Q}{\underline{Z}_{PQ}} \stackrel{!}{=} \frac{\underline{U}_P}{\underline{Z}_P} \quad \Leftrightarrow \quad \frac{\underline{Z}_P}{\underline{U}_P} = \frac{\underline{Z}_{PQ}}{\underline{U}_P - \underline{U}_Q} \quad \Leftrightarrow \quad \underline{Z}_P = \frac{\underline{Z}_{PQ}}{1 - \frac{\underline{U}_Q}{\underline{U}_P}} \tag{95}$$

$$\underline{I}_Q = \frac{\underline{U}_Q - \underline{U}_P}{\underline{Z}_{PQ}} \stackrel{!}{=} \frac{\underline{U}_Q}{\underline{Z}_Q} \quad \Leftrightarrow \quad \frac{\underline{Z}_Q}{\underline{U}_Q} = \frac{\underline{Z}_{PQ}}{\underline{U}_Q - \underline{U}_P} \quad \Leftrightarrow \quad \underline{Z}_Q = \frac{\underline{Z}_{PQ}}{1 - \frac{\underline{U}_P}{\underline{U}_Q}} \tag{96}$$

[8] **Association of Poles with Nodes:** Let's assume that a resistor R and a capacitance C are connected in parallel and one of the two pins is connected to a node and the other one is connected to ground, then the pole angular frequency can be written as: $\omega_{p_i} = \frac{1}{R \cdot C}$ [5, p. 509]

B.2. Miller-Effect and Multiplication

Let's consider an amplifier and an impedance connected between two nodes P and Q. By applying Miller's Theorem, the circuit can be redrawn as shown in Figure 31.

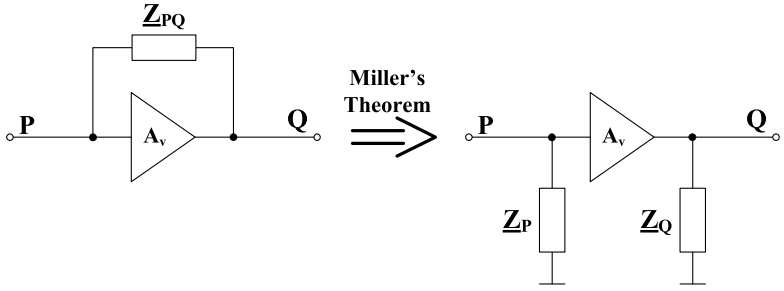

Figure 31: Conversion of a feedback impedance into two grounded impedances

By further investigation of equation 95, it is visible that the denominator of the impedance expression $\underline{Z}_P$ contains the transfer function of an amplifier ($\underline{A}_v = \frac{\underline{U}_Q}{\underline{U}_P}$). Equation 96 contains the reciprocal transfer function of an amplifier ($\underline{A}_v^{-1} = \frac{\underline{U}_P}{\underline{U}_Q}$). So equation 95 and 96 can be rewritten as follows:

$$\underline{Z}_P = \frac{\underline{Z}_{PQ}}{1 - \frac{\underline{U}_Q}{\underline{U}_P}} = \frac{\underline{Z}_{PQ}}{1 - \underline{A}_v} \tag{97}$$

$$\underline{Z}_Q = \frac{\underline{Z}_{PQ}}{1 - \frac{\underline{U}_P}{\underline{U}_Q}} = \frac{\underline{Z}_{PQ}}{1 - \frac{1}{\underline{A}_v}} \tag{98}$$

In summary, an impedance $\underline{Z}_{PQ}$ tied between the input and output of an amplifier with voltage gain A_v, gets decomposed into two grounded impedances which are multiplied by specific factors. The factor $1 - \underline{A}_v$ is called **Miller-Multiplication** [5, p. 512].

If the feedback impedance $\underline{Z}_{PQ}$ is purely capacitive, the equivalent input capacitor increases for inverting amplifiers. The feedback capacitor C_F gets Miller-multiplied at the input-terminal (see Figure 32).

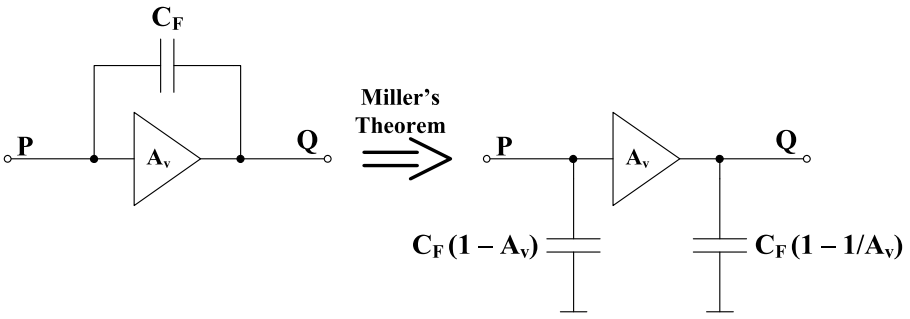

Figure 32: Miller-multiplied feedback capacitance

C. The Bipolar Junction Transistor at High-Frequency

So far, we used the low-frequency model of the BJT for circuit analysis. At the high-frequency domain, the model of the BJT will not stay the same. Obviously, several parasitic capacitors are influencing the BJT behaviour, which is shown in Figure 33. Those parasitic capacitors are intrinsic capacitors of the BJT which are related to the pn-junctions. Figure 34 shows a pnp transistor and the corresponding parasitic capacitors, which are not neglectable in high-frequency analysis.

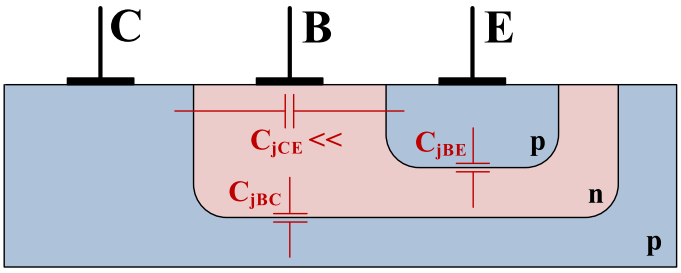

Figure 33: Cross section of a pnp-transistor

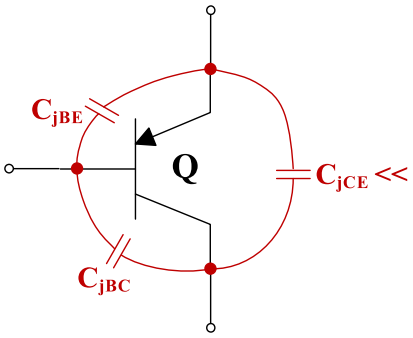

Figure 34: A pnp-transistor with parasitic capacitors

Compared to the two junction capacitances C_{jBE} and C_{jBC}, the junction capacitance C_{jCE} is negligible. This is due to the fact that there is a proportionality between the capacitance value and the geometry (The following applies to a plate capacitor: $C \propto \frac{1}{d}$). A closer look at the cross section, shown in Figure 33, shows that between the collector and emitter terminal a quasi series connection of two junction capacitances is appearing. So it is clear that this junction capacitance C_{jCE} has to have a smaller value than the two remaining ones.

D. Common-Base Stage with respect to the Miller-Effect

We will see in this section that the pnp-common-base transistor circuit, shown in Figure 1, is a special circuit with respect to the Miller-Effect.

With the knowledge of the small-signal circuit of section 3.6 and the parasitic capacitors of section C, which are important for the high-frequency perspective, we get the below depicted small-signal circuit (see Figure 35).

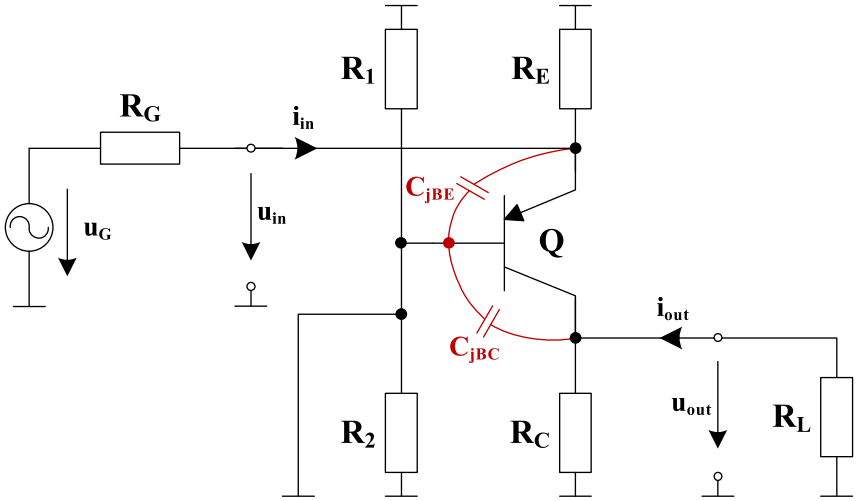

Figure 35: Small-signal circuit with parasitic capacitors

After some rearrangement of the circuit, shown in Figure 35, the final small-signal circuit is given in Figure 36. Undoubtedly, there is no capacitor tied between the input and the output of the pnp-common-base transistor circuit (amplifier). Due to that, the circuit is Miller-Effect independent. In addition, no parasitic capacitor gets Miller-multiplied. This fact gives the common-base stage the advantage that it suits best for high-frequency applications. For high-frequency applications, impedance matching is crucial. Bear in mind that the input impedance has to match the wave-impedance of a connected cable, wire or microstrip antenna (antenna on a printed circuit board).

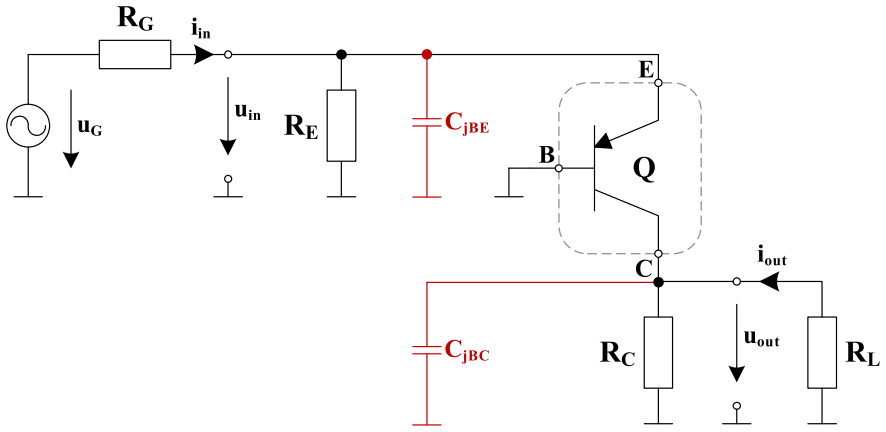

Figure 36: Simplified small-signal circuit with parasitic capacitors

E. LTspice Simulation Results

This section presents the LTspice® simulation results. The simulation software LTspice is used for checking the hand-calculated values against the simulated ones. For simulating the pnp-common-base transistor circuit, which is depicted in section 1.1, a spice model for the pnp transistor is required. Therefore, pnp spice model of Philips is used [13].

E.1. Operating Point Simulation

To simulate the operating point **OP** we have to use the LTspice spice directive **.op**. Figure 37 shows the schematic, which is used for simulating the operating point. Bear in mind that the signal source **uG** is switched off for this kind of simulation.

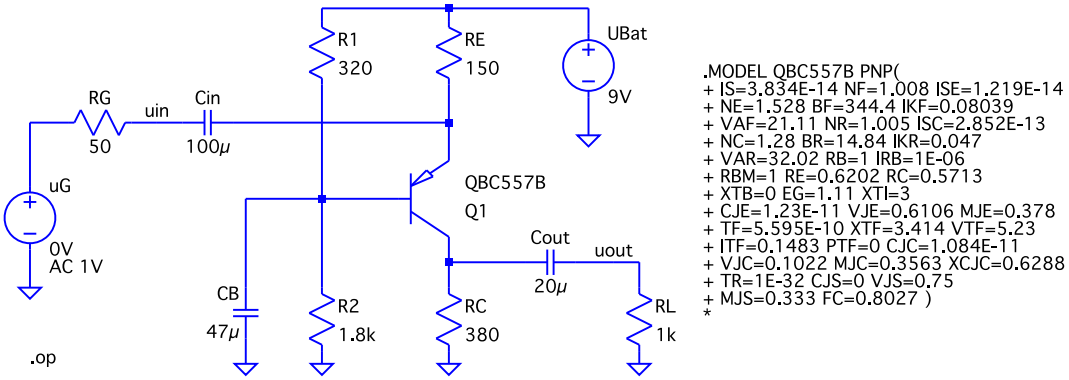

Figure 37: LTspice - schematic for operating point simulation

Figure 38 below compares the hand-calculated against the simulated voltage operating point values. The figure highlights that only minor differences exist between the simulated and the hand-calculated values. This is due to simplifications and linearisation of the circuit.

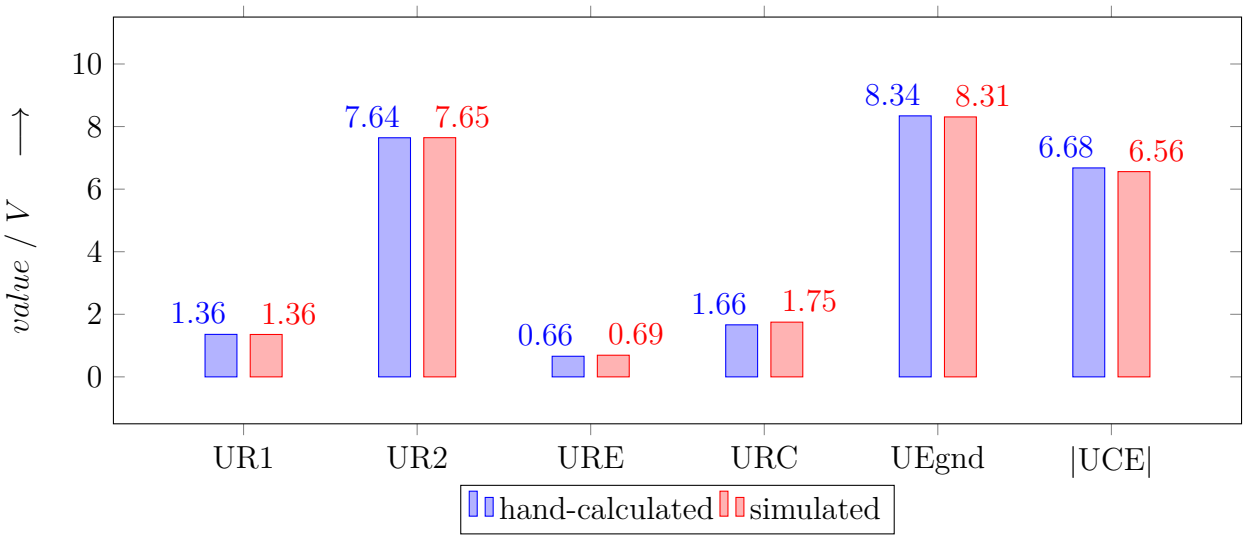

Figure 38: Comparison of calculated and simulated voltage DC-points

Figure 39 below compares the hand-calculated against the simulated current operating point values. As mentioned on the previous page, the figure highlights that only minor differences exist between the simulated and the hand-calculated values. This is also due to simplifications and linearisation of the circuit.

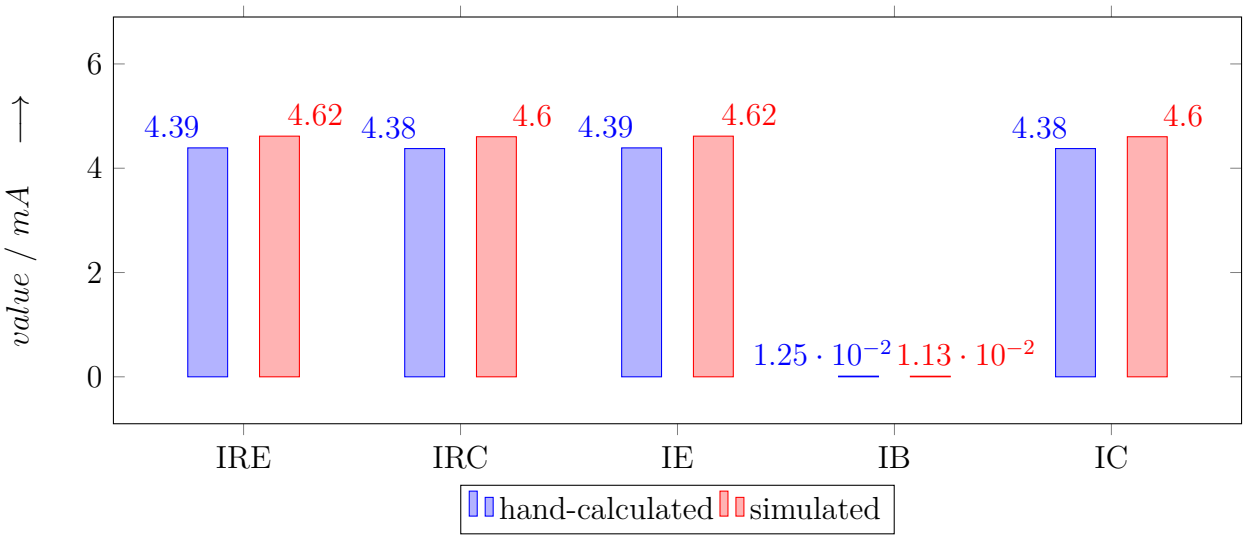

Figure 39: Comparison of calculated and simulated current DC-points

E.2. Time-Domain Simulation

As the name suggests, the time-domain simulation (spice directive **.tran**) focuses on signal changes, which means that the time-dependent influences are recorded. The time-domain simulation it is suitable for analysing the small-signal behaviour of a transistor circuit.

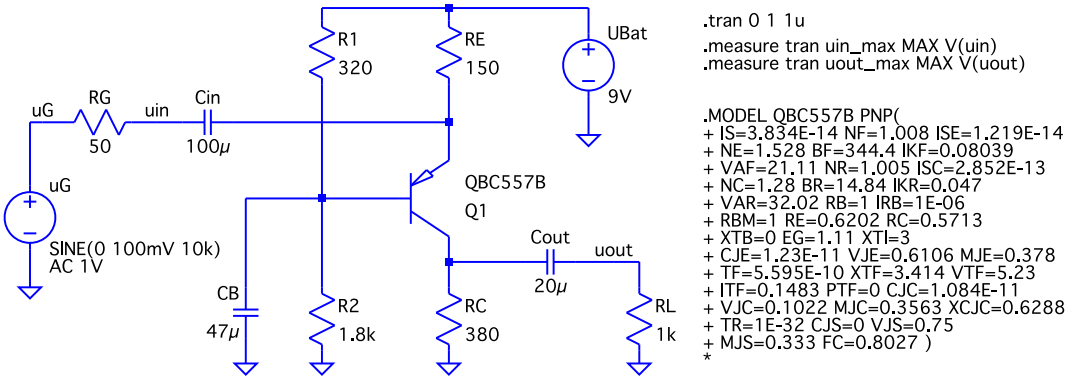

Figure 40: LTspice - schematic for time domain simulation

To determine the voltage gain of the above depicted schematic (see Figure 40), the peak value of the input $\hat{U}_{in}$ and output $\hat{U}_{out}$ voltage is monitored, which is shown in Figure 41. Bear in mind that the signal source **uG** has to have a signal frequency which is within the operating bandwidth of the circuit. For that reason, we have to keep the cut-off frequencies of section 4.2.6 in mind. Depending on the chosen signal frequency, the stop time and the simulation time-step has to be adjusted.

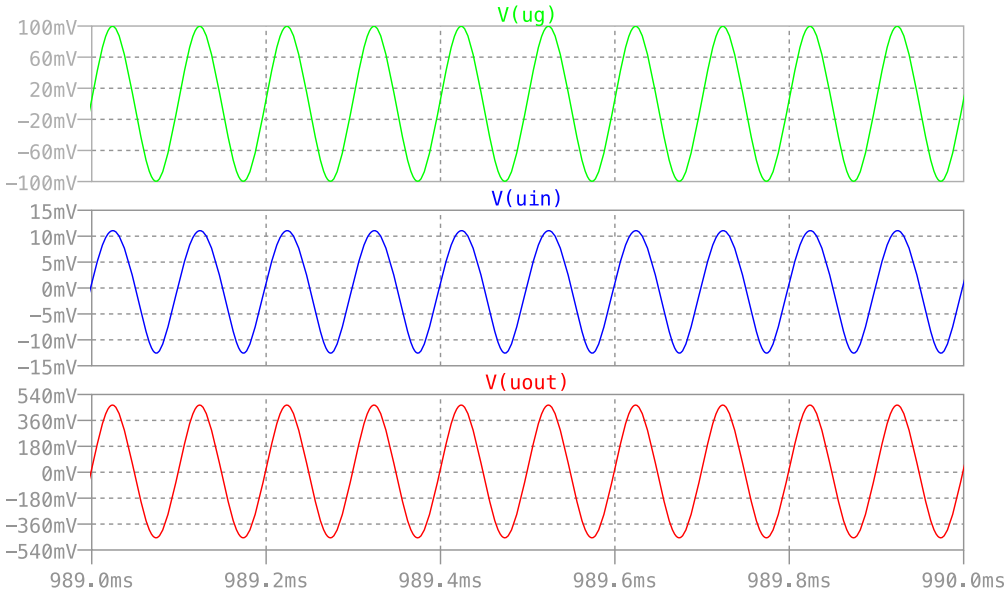

Figure 41: LTspice - time domain simulation result

Out of the above depicted plot we are able to determine the low-frequency voltage gain.

$$V_u = \frac{\hat{U}_{out}}{\hat{U}_{in}} = \frac{471.12\ mV}{11.06\ mV} = 42.6 \tag{99}$$

E.3. Frequency-Domain Simulation

The frequency-domain simulation (spice directive **.ac**) is an analysis concept for simulating the circuit behaviour with respect to various frequencies. The frequency-domain simulation is used for generating a Bode-Plot (magnitude and phase response).

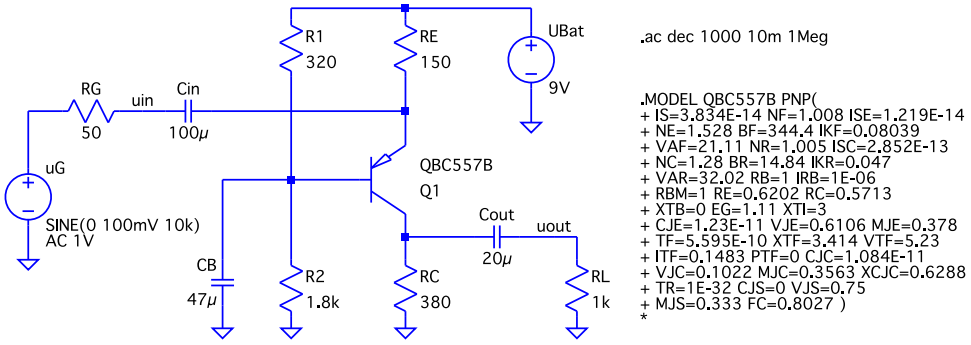

Figure 42: LTspice - schematic for frequency domain simulation

By sweeping the input signal frequency and recording the input u_{in} and output voltage u_{out} of the circuit, which is shown in Figure 42 above, the bode-plot, shown in Figure 43, is generated. The magnitude response is related to the ratio of the absolute value of input to output voltage. Whereas, the phase response is the argument of the ration between input to output voltage. For better representation the magnitude response gets plotted in a double logarithmic scale. In contrast to the magnitude response, where the abscissa and ordinate is represented in the logarithmic scale, for the phase response only the abscissa gets represented in the logarithmic scale. The simulated Bode-plot in Figure 43 (red trace) matches the hand-calculated ones (blue trace) of section 4.1.2 and 4.2.6 pretty good.

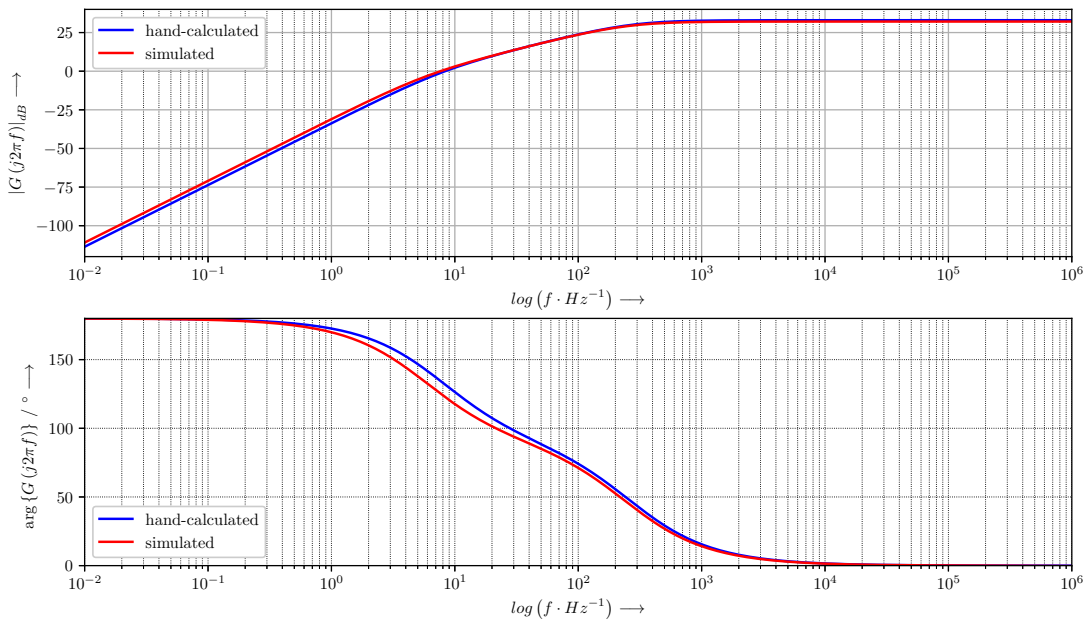

Figure 43: LTspice - frequency domain simulation result

E.4. Simulation of Input-Terminal Resistance and Voltage Gain

To evaluate if the small-signal input-terminal resistance r_{in} and voltage gain V_u of section 3.7.1 and 3.7.2 are calculated correctly, the small-signal equivalent circuit, which is shown in Figure 44 below, gets simulated via **LTspice**.

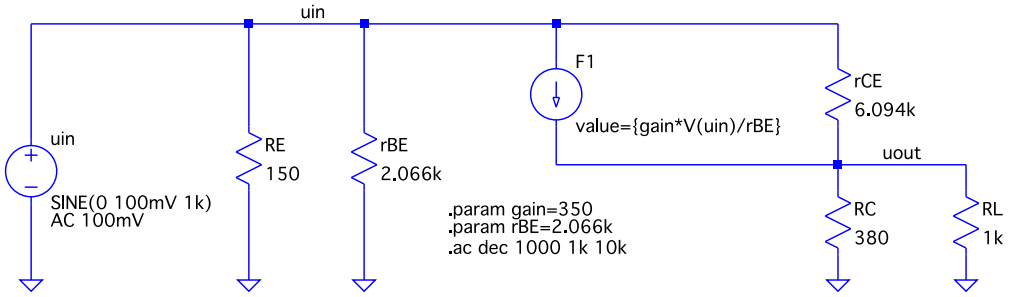

Figure 44: LTspice - schematic for input terminal resistance r_{in} and voltage gain V_u determination

Due to the fact that the above depicted circuit contains only linear components, the simulation can be done via the **.ac** analysis. The **.ac** analysis is conceived for linear frequency dependent circuits. In contrast to the time-domain simulation **.tran**, the frequency-domain simulation **.ac** gives an advantage in speed. Important to mention is the component **F1**, which represents a current-controlled current source **CCCS**.

Figure 45 below depicts the simulation result of the schematic, shown in Figure 44. It is visible in the lower Figure that the current **I(Uin)** has a negative sign. This due to the LTspice current directions. The current **I(Uin)** is flowing into the voltage source **uin**.

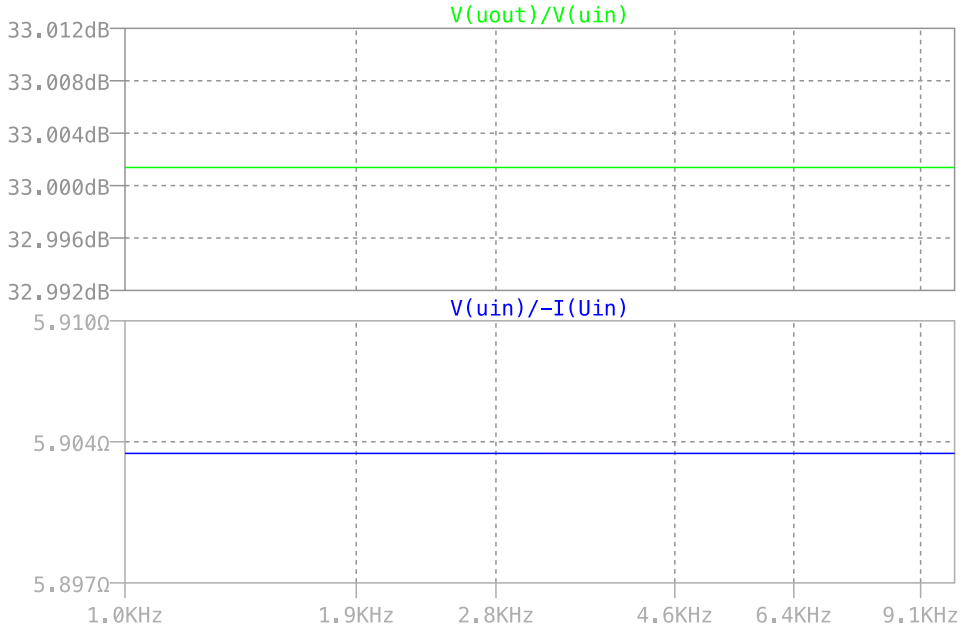

Figure 45: LTspice - simulation for input terminal resistance r_{in} and voltage gain V_u determination

E.5. Simulation of Output-Terminal Resistance

Analogous to section E.4 the small-signal output-terminal resistance r_{out} of section 3.7.3 can be evaluated by simulating the below depicted small-signal equivalent circuit (see Figure 46). Therefore, a voltage source **uout** is wired to the output terminal of the equivalent circuit.

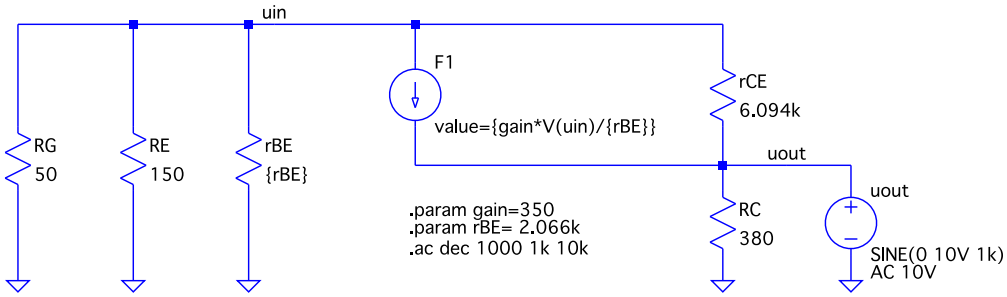

Figure 46: LTspice - schematic for output terminal resistance r_{out} determination

As mentioned in the previous section, the above depicted circuit, shown in Figure 46, contains only linear components. Due to the fact, that the circuit contains only resistors it is predictable that no transient behaviour will appear. For that reason, the circuit can be simulated over frequency. This gives the advantage to reduce simulation time. The simulation results from the circuit, shown in Figure 46, are depicted in Figure 47 below. Furthermore, the plot below shows that the current **I(Uout)** has a negative sign. This due to the LTspice current directions, which we mentioned in previous section E.4. By comparing the calculated value of the output-terminal resistance r_{out} of section 3.7.3 with the simulated one below, it is visible that they are more or less equal.

Figure 47: LTspice - simulation for output terminal resistance r_{out} determination

F. Overview of Basic Transistor Amplifier Circuits

Bipolar and MOS transistors are capable of providing useful amplification in three different configurations. In the common-emitter or common-source configuration, the signal is applied to the base or gate of the transistor and the amplified output is taken from the collector or drain. In the common-collector or common-drain configuration, the signal is applied to the base or gate and the output signal is taken from the emitter or source. This configuration is often referred to as the emitter follower for bipolar circuits and the source follower for MOS circuits. In the common-base or common-gate configuration, the signal is applied to the emitter or the source, and the output signal is taken from the collector or the drain. Each of these configurations provides a unique combination of input resistance, output resistance, voltage gain, and current gain. In many instances, the analysis of complex multistage amplifiers can be reduced to the analysis of a number of single-transistor stages of these types. [11, p. 173-174]

It depends on the application field which type of transistor and transistor circuit fits best for the respective application. The table 6 below gives a brief overview of some essential parameters for the three different basic transistor amplifier configurations.

Table 6: Comparison of the three basic transistor amplifier circuits [2, p. 889]

Characteristic	***Common Base***	***Common Emitter***	***Common Collector***
input terminal resistance r_{in}	(low)	(moderate)	(high)
output terminal resistance r_{out}	(high)	(moderate)	(low)
phase inversion	(no)	(yes)	(no)
voltage gain A_v	(high)	(high)	(low)
current gain β	(low)	(moderate)	(moderate)

G. Transformation Concept for Sinusoidal Signals

In this section a transformation concept for sinusoidal signal will be presented. The reason why we want to transform sinusoidal signals is due to trigonometric functions.

Equation 100 below is representing the transformation concept of sinusoidal signals between the time- and frequency-domain. This allows to solve linear circuits without having to deal with trigonometric functions.

$$\begin{aligned} u(t) &= \hat{U} \cdot \sin(\omega t + \varphi_u) = \Im\{\underline{u}(t)\} = \Im\left\{\hat{U} \cdot e^{j(\omega t + \varphi_u)}\right\} = \Im\left\{e^{j\omega t} \cdot \underbrace{\hat{U} \cdot e^{j\varphi_u}}_{\underline{U}}\right\} \\ &= \Im\left\{e^{j\omega t} \cdot \underline{U}\right\} \\ i(t) &= \hat{I} \cdot \sin(\omega t + \varphi_i) = \Im\{\underline{i}(t)\} = \Im\left\{\hat{I} \cdot e^{j(\omega t + \varphi_i)}\right\} = \Im\left\{e^{j\omega t} \cdot \underbrace{\hat{I} \cdot e^{j\varphi_i}}_{\underline{I}}\right\} \\ &= \Im\left\{e^{j\omega t} \cdot \underline{I}\right\} \end{aligned} \tag{100}$$